The 8 bits 100 MS/s Pipeline ADC for the INNOTEP Project – TWEPP-09

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Abstract

This paper describes the Analog to Digital Converter developed for the front end electronic of the IN2P3 INNOTEP project by the "pole microelectronique Rhone-Auvergne". (Collaboration between LPC Clermont-Ferrand and IPNL Lyon). This ADC is a 4 stages 2.5 bits per stage pipe line with open loops track and holds and amplifiers. It runs at 100MSamples/s and has 8 bits resolution. The stages used two lines, the gain line and the comparison line, with most operators running in current. The main idea of this current line is to make a first step toward an all in current structure. Currently, this ADC is designed with a 0,35µm SiGe technology.

I. INTRODUCTION

Positron Emission Tomography (PET) scanners have been recognized as very powerful and sensitive instruments for biomedical purposes such as brain studies, cardiac imaging, early cancer diagnosis and therapy. They operate by indirect detection of radioisotope's positron emission, which annihilates with an electron to produce a pair of 511-KeV (gamma) photons emitted in opposite directions. Each escaped photon may hit a scintillator to generate a light pulse that can be detected using a photomultiplier tube (PMT) or an avalanche photodiode (APD). Via sensitive and rapid detection of the 511-KeV photon pair, the positron annihilation event can be localized on a straight line of coincidence (line of response, or LOR). PET scanners should make use of low-noise and rapid electronics associated with PMT or APD. The associated electronics may include successive charge-sensitive amplification, analog filtering, A-to-D conversion and digital signal processing, as shown in Fig 1.

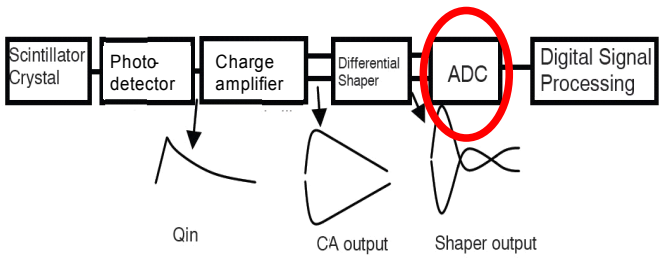

Figure 1: Architecture of the detector-associated electronics

We present in this paper the design of an Analog to Digital Converter for this application. The proposed circuit is based on a fully differential structure.

II. CIRCUIT DESCRIPTION

The architecture chosen is a 4 stages pipe line (seen in fig2). Each stage is designed in 2.5bits to get a resolution of 8 bits. There are 6 comparators per stage (for 7 references). The Analog to Digital Converter consists of two parts: the gain line which is fully differential and open loop, to try to minimize the stability problems, and the comparison line using current structure, to limit the comparators kick back noise and charge injection in the 3 bits DAC. The first three stages are similar, only the 4th stage is different, there is no gain line. The constraints of quality are released by a factor 4 between the stage n and the stage n +1.

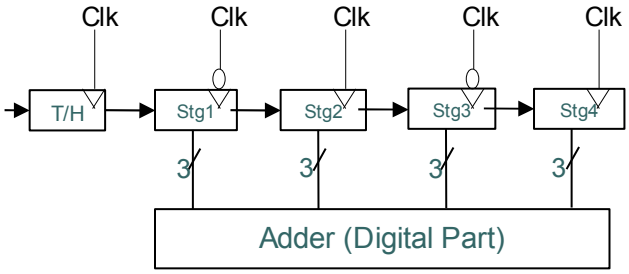

Figure 2: The ADC architecture

III. Characteristics and tolerances

For the first version, the clock was different for the 4 stages (Clk for stage 1 and 3, and reverse Clk for stage 2 and 4). We obtain new bits every 5ns, at a real rate of 200MHz at the outputs of stages.

A behavioral structure was made to determine the critical point of the structure studied. After simulation the following results were found:

- The need of a comparator with important gain.
- Comparators offset uncritical (1/16 of dynamics => 125mV).
- Quality of references and amplifiers is a key point (+/- 2LSB) in the first stage.
- The maximum gain error to be tolerated is of 4%.

IV. The structure of the ADC

A. Gain line

The gain line in the first version is structured with a single track/hold and a subtraction block. To obtain the necessary gain of 4 for the 2.5 bits structure, these two blocks have an intrinsic gain of 2. The Track / Hold and the subtractor use an open-loop structure and bipolar transistors to obtain the expected 100MHz. The subtraction is done using a DAC working in current mode which controls the current generators associated with the input differential pair.

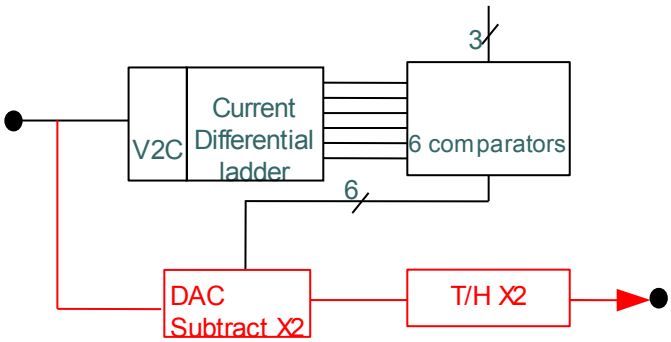

Figure 3: The stage structure, with the comparison line (in black) and the gain line (in red)

B. Subtractor with gain 2

One interesting feature of this block, due to the distribution of the gain 4 between the two blocks on the gain line, is that the output voltage is the half of the dynamic (1V differential), simplifying the excursion problems. However, it calls for a better precision.

The gain 2 differential multiplier is a classic open-loop structure that uses a resistor ratio. A single-stage correction is implemented to obtain the absolute accuracy requested. To perform the subtraction we use variation of currents between the two branches of the differential multiplier.

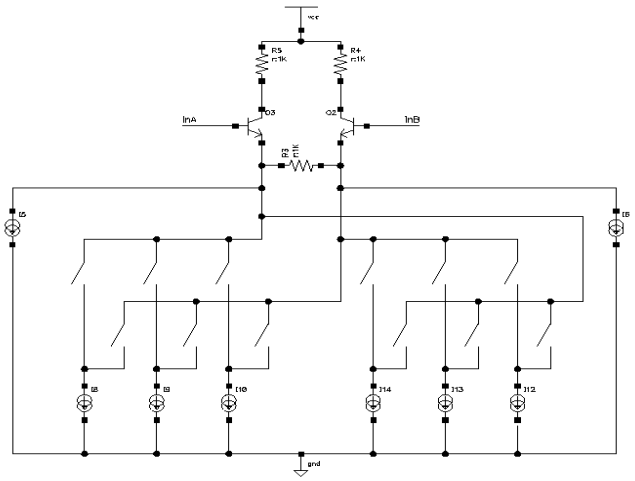

Figure 4: The subtractor structure, with the gain 2 differential amplifier and the current DAC structure. Depending on the results of the comparisons, the generators are distributed separatly on one of the two branches.

In fact, the current in each branch is defined by a DAC of which switches are controlled by the outputs of the comparators of the same stage. Another key feature of this structure is to work at constant current and to avoid the classical voltage references.

1) *Multiplication:*

A classic gain 2 differential amplifier in open-loop is operated for the multiplication. Corrections have been simplified to the maximum as we have half of the dynamic on the output: fixed gain, improved gain for large signals by a diode which decreases a part of the collector resistor and the structure is accelerated using a capacitor in parallel with the collector resistor.

2) *Current Digital to Analog Converter:*

The subtraction of references is made implementing a DAC in current, using a basic structure which that adds current generators to convert the input voltage. With the subtraction by modulation of current in the differential branches, we achieved:

- no external references (only one current source and w/l for all generators).
- direct use of the comparators output.
- easier control of charge injection phenomena.
- better linearity.

This structure operates with 8 current generators, there is 2 fixed generators and we have to control the other 6 identical generators. Through the DAC, which uses a system of switches, the current generators are distributed in both branches, which will allow us to perform the subtraction.

For a zero subtraction (range 0), currents should be identical in the two branches, or a distribution 3-3 for the generators. Then we have 4-2 (a difference of 2 units of current) for the range 1 and 5-1 (a difference of 4) for the range 2 and 6-0 (a difference of 6) for the range 3. We get the opposite for the other 3 ranges. (-3, -2 and -1)

We have staggered the different ranges -3, -2, -1, 0, 1, 2, 3 which will allow us to obtain the good references for the subtraction depending on the input voltages.

C. track and hold (gain 2)

On the output of each stage, we put a track/hold of gain 2. The input level is identical for all blocs: 2.3 V. The design is very classic: adaptation of the input level, gain 2 amplifier in open-loop with its corrections, adaptation level, exit on switches, storage capacitors and output transistors (PMOS needed to get the right common mode voltage).

The signal remains on PMOS therefore there is no current discharging the capacitor. The noise depends only on the capacitor value: $\sigma = kT/C$, we want the σ less than 0.25 LSB differential or 1mV. For the capacitor: $C > 20\ aF$ is needed, and finally a capacitor $C = 300\ fF$ have been chosen.

One critical point with this structure is the switches. The errors due to the switches need to be controlled: the charge injection and the clock feedthrough.

1) Amplification by 2:

We use the same structure as for subtractor amplifier, mounted in gain 2, but we do not use here an acceleration capacitor.

2) Switch:

The principle is to take a master transistor with a ghost transistor on each side controlled by the reverse clock. The most important point that needs to be controlled is the charge injection. We use NMOS because of the polarity of the signals. By testing, it appears that it is with ghost transistors of half the main that we get the best results. The minimum size of transistors to reduce the charge injection is operated. The best result in charge injection is achieved with w=10µm and l=0.35µm for the master, w=5µm and 0.5µm for the ghosts.

D. Comparison line

The comparison line is composed of 3 parts, the voltage to current conversion block, the differential current ladder and the comparators. The main interest of this line is the use of a differential current ladder.

E. Voltage to current conversion

This block was realised to modulate a quiescent current (in fact, we control current conveyor) according to the differential input voltage. Two correction structures which operate depending on the signal are implemented for the linearity. There is therefore a main floor with a fixed modulation using a parallel resistor set off by a pair of diodes. A second floor adds a little current, which is modulated by the same correction as the main floor (with different sizes of components). All floors use the same input voltage to 2.3V, this leads us to insert an input stage to the voltage to current block (V2C).

To check the quality of the transformation, the outputs are converted into tensions with the transistors of the same size as the V2C, the current measurement is a voltage generator to the same value as the input comparison voltage, and we consider an arbitrary gain of 1000; The simulation error is less than ± 0.5mV for a LSB of 8mV.

After the layout achievement, it appears that this floor is not fast enough for an important comparators changeover. It was accelerated with a capacitor and increasing the current. A linearity error of ± 1/4LSB is obtained, which is correct. We will have to edit the position of the comparators according to the errors of this blocks, this correction may include the V2C error. Anyway there is an important error margin on the comparator (because of the use of 2.5 bit structure), and it is the gain bandwidth product aspect of the whole comparison which is decisive.

F. The ladder

We now begin the current scales study. The first element is the comparator. In this structure, we fixed the comparator operating at zero differential voltage on a slave floor and, if possible, at the same common mode voltage regardless of the comparator. The size of resistors or transistors can either be adjusted, it was choosen arbitrarily to adjust the size of transistors.

1) Differential current ladder:

Determination of the current failover compare:

m: coefficient giving the current values.

In the master branches: $I_a = I_r \times (1 + m)$ *and* $I_b = I_r \times (1 - m)$ with k_a and k_b reports currents between masters and slaves.

In the slave branches: $I_A = k_a \times I_r \times (1 + m)$ and $I_b = k_b \times I_r \times (1 - m)$, the changeover tensions are the same in both branches, $R_A \times k_a \times (1 + m) = R_B \times k_b \times (1 - m)$

If one chooses $R_A = R_B$ (this is a possible degree of freedom): $k_a \times (1 + m) = k_b \times (1 - m)$

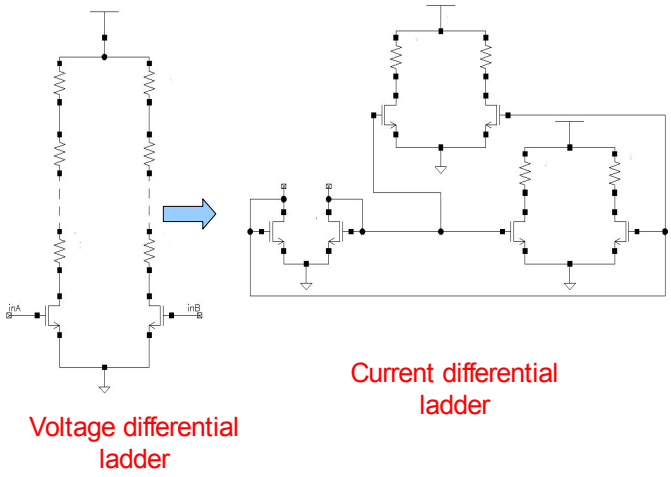

Figure 5: Passage of a resistances range asking for a very good linearity to 6 differential pairs using transistors with different W / L to set the comparators working point voltage.

We want to fixe the comparison level of different pairs at the same common mode voltage. $k_a \times (1 + m)$ must always have the same value, for example 1. k is the ratio w / l. we can write:

$$w_a = \frac{w}{1+m}$$

$$w_b = \frac{w}{1-m}$$

To achieve the design, the resistors R_A and R_B must be paired, but their absolute values is essential only for the operating point of the comparator. A good treatment is required, depending on the desired accuracy, the ratio of transistors w_a and w_b, largely among themselves, the relationship with the masters will play on the working point of the comparator. Care matching: master transistors with them, the resistance between them, the size ratio of transistors slaves. The absolute value of these components will play on the comparators working point voltage.

Using this current scales help us to control the kick back noise. If 6 different comparators on one differential pair are operated, the kick back noise generated by the different comparators is absorbed by the single differential pair. With this current scales, the comparators are all identical, and the kick-back noise generated by the comparator is absorbed with this structure by 6 differential pairs.

G. The latched comparator

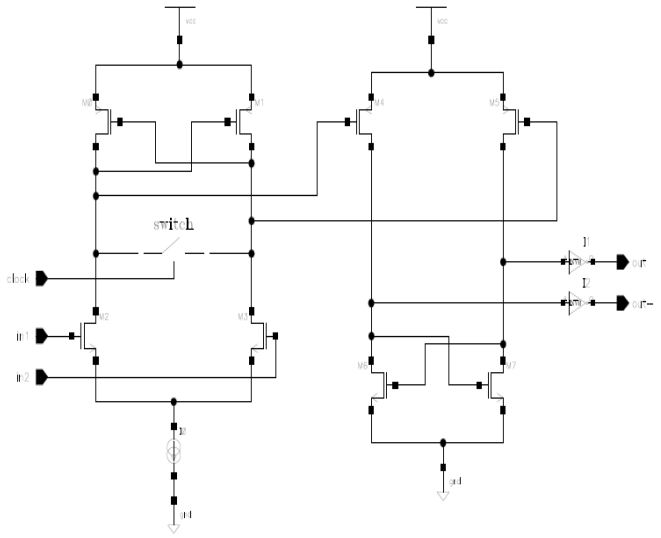

Figure 6: The diagram of the latched comparator

Following a design now often implemented, we have made the comparator faster to keep the 100MHz. The schematic concept is illustrated in Fig 6. In the design, a problem of product gain-bandwidth which need to be improved is encountered, it is necessary to optimize the assembly with this point of view. Moreover, if we consider the design of Fig 5, the signal pass in current before the latched comparator, we look for the next version, the possibility of designing this comparator also all in current.

V. Corrections to the ADC structure

A. Timing management

In the first version of the ADC, when there is an important change in the input voltage, the subtractor have not enough time to do the multiplication and references subtraction. More exactly, the subtractor have less than 5ns to obtain the good value. To remedy this, without touching the opening time, we doubled the time during which the subtractor may work. The clock is now the same for the 4 stages. We obtain new bits every 10ns, at a real rate of 100MHz in the output of the stage. It can be possible because we have chosen to use two T / H on each stage. The comparison order is fixed at the end of the track period of the output T/H on the preceding stage. The possible range change have therefore a complete period (the track and hold the T / H input) to be realised, 10ns exactly. This timing is now used and allows the floor the more critical (subtract X2) to manage the range change.

On the input of the comparison line, we therefore place a track/hold gain 1 in order to double the working time of the subtraction block.

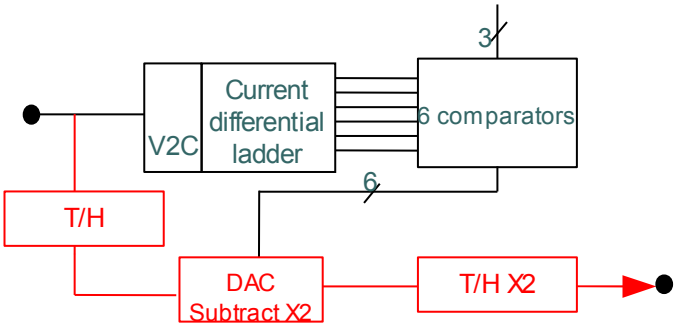

Figure 7: The stage structure with the T/H at the entry of the gain line

B. Digital Part

The ADC digital part is the adder, which has been synthesized and developed/routed to be implemented in parallel with the analog part. Check inputs/outputs have been built on this block, that can help us to trace the possible conversion errors at the different stages.

VI. Simulations

Different schematic simulations were made, the bandwidth was the critical point with this structure. The process/matching simulation gave results corresponding to specifications, with a gain error and offsets level lower than the tolerances given by the behavioral simulations. After the layout achievement, parasitic simulations were made, we use the capacitor extraction, to check if the bandwidth is not too decreased. In Fig 8, we can see that we obtain ideal results.

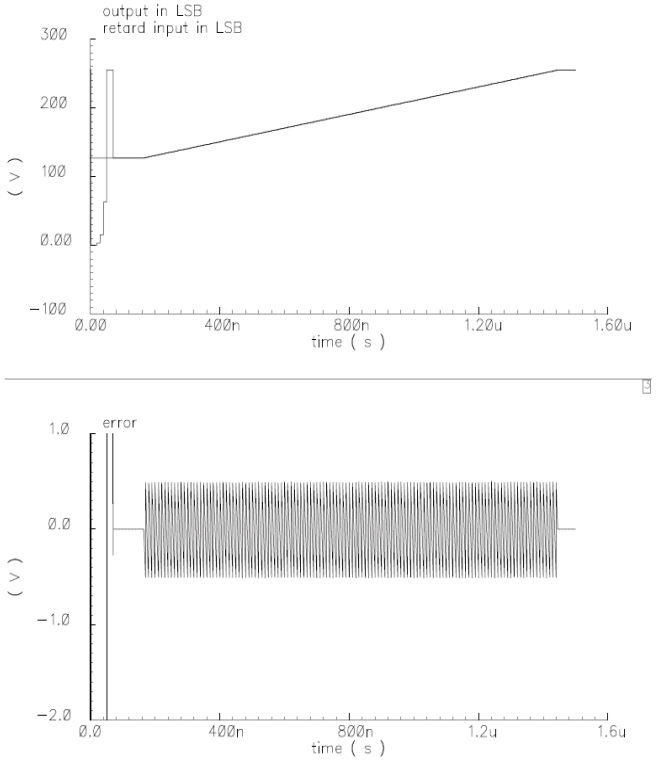

Figure 8: Results with parasitic simulations, we obtain ideal results. We generated a ramp at the input of the ADC and then compare the conversion results with this ramp.

VII. Measurements

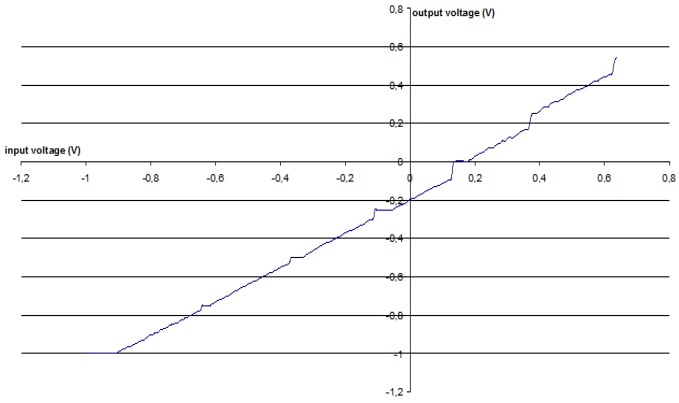

Figure 9: ADC output (in V) according to a ramp in input (in V)

On the graph, a conversion error is present all along the ramp because an offset is present at the output of each stage. Levels are also visible (first stage levels), the 2.5-bit algorithm does not compensate for this offset.

From -0.91 V to 0.15 V in input, the ADC, despite the offset and levels, offers interesting results. In fact, it works on this voltage range at 100MHz and with a precision of 9 bits (we use the 9th bit due to the use of 2.5bits algorithm). The INL (when we take into account gain and offset errors) is less than 1LSB, as the noise.

All the chips had this error and gave almost identical results, so we were routed to an error in the layout. After a complete study to determine where this offset error came from, we found that in the layout of subtract X2, a parasitic resistance injects an error in the half of current generators.

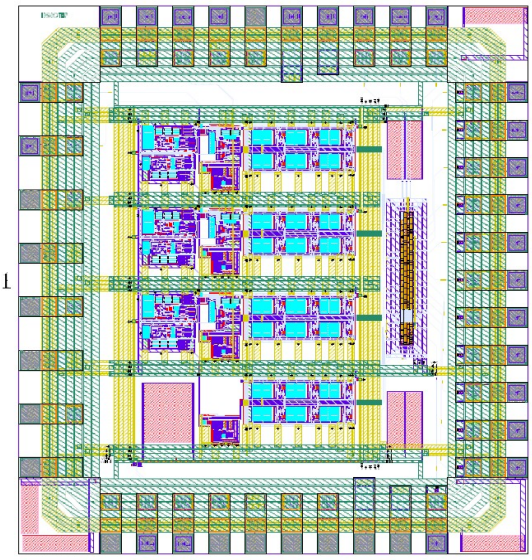

Figure 10: The layout of the ADC

This parasitic resistor less than 5 ohms had not appeared on the old parasites simulations (less accurate). With this resistor, we have an offset of more than 250mV at the output of the stage. After correcting the offending tracks, the layout is fixed, and we hope that the next foundry will be satisfactory. Moreover, process/missmatch problems seem to be mastered because we obtain the same results for all chips.

Table 1: Features of the ADC

Architecture	2.5-bit/stage
Technology	0.35µm SiGe
Area	2425 µm x 2775 µm
Supply Voltage	3.5 V (Analog), 3.3 V (Digital)
Resolution	8 bits (9 bits possible)
Full Scale	2V differential
Conversion rate	100MS/s
Consumption	240mW
INL	<1LSB

VIII. CONCLUSION

A pipeline ADC has been designed using the 0.35 µm BiCMOS technology of Austriamicrosystems. It presents a resolution of 8 bits with a clock frequency of 100MHz. The power consumption is 240mW with a power supply of 3.5V. The performance of the ADC has been measured. Currently, this first prototype does not respect the specifications. But the offset error have been corrected and a new prototype will be sent before the end of the year. This first prototype give us some satisfactions:

- It works at 100MHz
- Current driven blocks works perfectly (comparison levels errors < 1 LSB)
- The yield seems to be good

IX. References

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