3D electronics for hybrid pixel detectors – TWEPP-09

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Abstract

Future hybrid pixel detectors are asking for smaller pixels in order to improve spatial resolution and to deal with an increasing counting rate. Facing these requirements is foreseen to be done by microelectronics technology shrinking. However, this straightforward approach presents some disadvantages in term of performances and cost. New 3D technologies offer an alternative way with the advantage of technology mixing.

For the upgrade of ATLAS pixel detector, a 3D conception of the read-out chip appeared as an interesting solution. Splitting the pixel functionalities into two separate levels will reduce pixel size and open the opportunity to take benefit of technology's mixing. Based on a previous prototype of the read-out chip FE-I4 (IBM 130nm), this paper presents the design of a hybrid pixel read-out chip using three-dimensional Tezzaron-Chartered technology. In order to disentangle effects due to Chartered 130nm technology from effects involved by 3D architecture, a first translation of FE-I4 prototype had been designed at the beginning of this year in Chartered 2D technology, and first test results will be presented in the last part of this paper.

I. INTRODUCTION

Improving spatial resolution and dealing with higher luminosity and radiation's levels is one of the challenges of the ATLAS read-out chip upgrade [1]. A way to decrease pixel size is to split pixel into two or more parts and to stack them vertically. By this way pixel area is roughly reduced by the number of stacked circuits. This architecture is made possible by new 3D technologies.

Tezzaron offers one of the first commercial processes for 3D integrated circuit. This process combines Chartered 130nm technology and Tezzaron 3D technology. A first MPW run for High Energy Physics has been organized within a consortium of 15 institutes (France, Italy, Germany, Poland, and United-States).

This paper presents one project submitted in this run, called FE-TC4 and designed in collaboration by Bonn, CPPM and LBL. Based on the FE-I4 prototype (pixel read-out prototype chip for ATLAS upgrades, in IBM 130nm [2]), FE-TC4 splits pixel functionalities into two levels. The first one (Tier 1) is dedicated to the analogue part of the pixel and for sensor connections and is described in section III. The second one (Tier 2) is dedicated to the digital part of the pixel. These two Tiers will be connected using 3D connections.

Two different designs were implemented for the digital Tier (Tier 2). The first one, detailed in section IV A, has been especially intended to study the parasitic coupling between Tiers. This Tier also provides some simplified data readout functionality. The second one, described in section IV B, is based on read-out structure foreseen for ATLAS pixel Front-End upgrade and includes “4-pixel region” architecture.

In order to evaluate 3D technology specific issues, 4 test circuits have also been designed and are developed in section VI. Specific issues like reliability of 3D connections and influence of these connections on transistors have been addressed.

The main objectives of FE-TC4 circuits are to demonstrate the feasibility of these new 3D hybrid pixel detectors, to measure the parasitic effects involved by 3D structure and to test the sensor hybridization on top of such circuit.

II. BRIEF DESCRIPTION

A. Vertical integration with 3D Tezzaron-Chartered process

3D technology has been initiated by the increasing demand of memory cells and by the idea to stack vertically memory on processor, allowing better access times. This implies to make connections on the top and on the bottom of each stacked circuit. For this run, two Tiers are stacked face to face, that is to say that transistors (top of individual circuits) face each other. This configuration implies connecting the sensor through the analogue Tier from the backside, and designing sensitive elements like preamplifiers in front of digital Tier parts. This “face to face” wafer to wafer bonding technology, imposed by the MPW run, is not the best way of interconnecting for our purposes.

Each of the stacked Tier can be accessed from their backside with use of Through Silicon Vias (also called Super-Contacts). Tezzaron process is based on a Via First technology: Super-Contacts are formed before the BEOL (Back End Of Line) of Chartered process. This kind of technology allows very small via dimensions and pitches. Super-Contacts are drawn with a diameter of 1.2µm and a minimum pitch of 2.5µm. As Super-Contacts can only be 12µm deep at most, wafers must be thinned in order to create through silicon connections.

A 2-Tier circuit is sketched in Figure 1, underlining the physical stack and the placement of Super-Contacts.

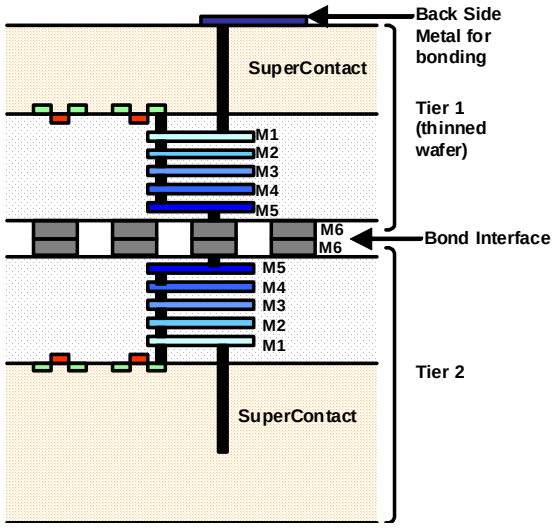

Figure 1: 3D assembling of 2 Tiers (not to scale)

Tiers are bonded wafer to wafer with Cu-Cu thermo-compression process by using the 6th metal layer of Chartered technology to form the bond interface.

This Bond Interface is formed by an uniform pattern of hexagonal metal shapes, as shown in Figure 2. In order to provide a strong mechanical coupling, this pattern covers completely the chip, and most of the interface bonds are not physically connected to an active signal. Electrically unused bonds are left floating.

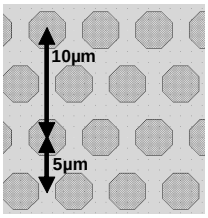

Figure 2: Bond interface layout

Furthermore, to allow the possibility of testing each Tier separately, IO pads for bonding or for probe testing can be re-formed above metal 6 (bond interface). This possibility is given by one additional metal level offered by Chartered technology and called Re-Distribution Layer (RDL). However wafers on which RDL metallization is done are lost for 3D hybridization because of masked Interface Bonds.

B. *FETC4 project description*

The full Chartered reticle size is 26mm by 31mm. This reticle has been shared between all MPW participants into sub-reticles (A to K) of 6.4mm by 5.5mm.

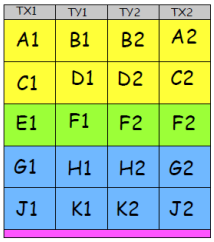

Figure 3: Entire Chartered reticle layout

A particularity of this project is to avoid the cost of two sets of masks by implementing the two Tiers in the same reticule whereas a conventional 3D structure stacks two different wafers (which can also be fabricated with different technologies). With only one set of mask, and by taking care of layout mirroring between the two Tiers, two identical wafers can be bonded together face to face. For example, sub-reticle A1 (top Tier) is bonded with A2 (bottom Tier), and B1 is bonded with B2.

When the 4 sub-reticles (A1, B1, A2 and B2) are bonded face to face, four 3D-chips are formed: A1 on top of A2, B1 on top of B2, but also A2 on top of A1 and B2 on top of A1. As only the top Tier will be thinned, the two last configurations are uninteresting because super-contacts of A1 and B1 chips cannot be accessed. The disadvantage of this choice is to lose the half of 3D chips.

Sub-reticles reserved for FE-TC4 project are C1, C2, D1 and D2. As presented in Figure 4, they contain the following circuits:

- AE : Tier 1, analogue chip FE-TC4-AE
- DC : Tier 2, digital chip FE-TC4-DC (« à la FEI4 »)
- DS : Tier 2, digital chip FE-TC4-DS (for parasitic coupling study)
- C1-1, C1-2, C1-3, D1-1, D2-1, C2-1, C2-2, C2-3 : Test circuits
- SEU : Test circuit for SEU studies
- "α" area : Reserved for another project

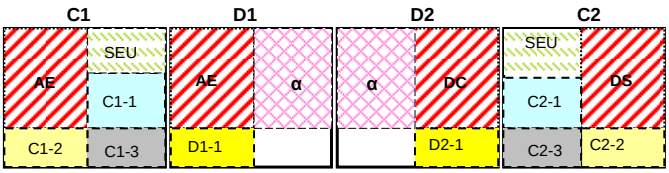

Figure 4: FE-TC4 sub-reticles

III. Tier 1 : Analogue Design

A. *Analogue Tier 1 design strategy*

A first translation of FE-I4-P1 prototype chip from IBM 130nm to Chartered 130nm technology had been performed in February 2009 with the design of FE-C4 prototype (Chartered 2D technology with 8 metal levels). Based on this first step, FE-TC4-AE analogue Tier chip has been designed in Tezzaron-Chartered 3D technology with 5+1 metal levels. The pixel size, for this attempt, is also kept identical to FE-I4-P1 pixel: 166µm x 50µm.

This Tier is pin to pin compatible with FE-I4-P1 circuit, even if some subsidiary elements have not been implemented. Without these elements, some of the I/O pads remain unused. In the 3D structures, I/O signals of Tier 2 are transmitted through the Tier 1 (where some pads must be included on the back-side for IO connections), these unused pads are reserved for Tier 2 signals or powers. These "digital" pads are not connected to the analogue Tier 1 core. They only transmit

signals through Tier 1, from bond interface to back-side metal.

At the schematic level, the analog Tier of FE-TC4 is identical to the FE-C4 prototype designed in Chartered 2D technology earlier, as well as to the previous IBM prototype FE-I4-P1. Components (transistors, resistors…) for Chartered design have been chosen as close as possible of components used in IBM design. Because of the tight schedule for these runs, no optimization of transistors has been made.

3D Tezzaron/Chartered run is limited to 5 metal levels for routing, plus a 6th level reserved for bond interface. From the FE-C4 design, the FE-TC4 was redesigned by:

- Reducing the number of metal layers in layout,
- Adding all 3D connections:
  - for the input signal from sensor,
  - for the output signal to Tier 2.
- Changing 2D I/O pads into 3D I/O pads.

Reducing the number of metal layers is possible for this chip because the matrix is only of 14 columns of 61 pixels. But for larger matrix, power distribution must be thought through again. One possible solution can be to use metal levels of Tier 2 for Tier 1 power routing.

B. *Analogue pixel with 3D connection*

The most time effective approach has been adopted. Pixel schematic is kept identical to FEI4-P1 pixel with amplifiers, discriminator, DACs, configuration registers and simple read-out part. Specific changes have been implemented for 3D assembling:

- Input metal contact for sensor hybridization is routed by Super-Contacts to Tier 1 back-side.
- An electrical contact using interface bonds has been added to route the discriminator output signal to the digital Tier (Tier 2).
- One switch and its configuration signal has been added to transmit the discriminator output signal either to Tier 2, either to simple read-out part existing yet into the pixel. Figure 5 indicates the location of this switch in the pixel schematic.

With these changes, pixel output signal can be read-out, either by the same way than FE-I4-P1 and FE-C4 pixel (in this case, Tier 2 is not needed), either through the Tier 2 chip.

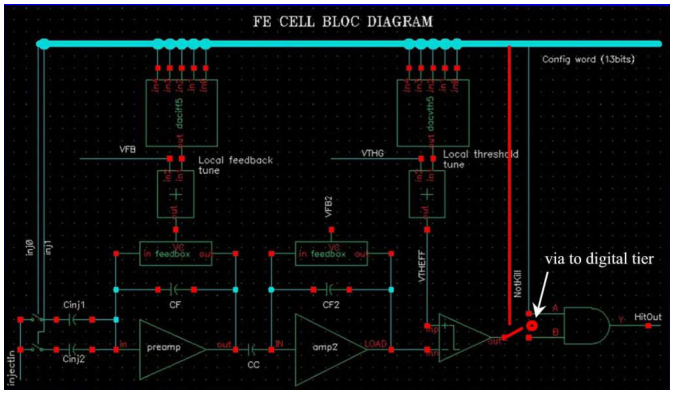

Figure 5: Pixel structure with switch for 3D connection

IV. Tier 2 : Digital Design

The analogue Tier 1 output is read-out by the digital Tier 2. Two versions have been designed for this digital chip. The first is intended to study parasitic coupling effects between the two Tiers in order to test 3D architecture related issues. This chip is called FE-TC4-DS. The second version called FE-TC4-DC is a more complex read-out chip which structure is close to the one foreseen for FE-I4.

A. *FE-TC4-DS :Tier 2 dedicated for test*

In 2D pixel designs, care is taken to avoid parasitic coupling between analogue and digital signals. One of the way used is to implement analogue and digital part as far away from each other as possible in the pixel area. In such a 3D arrangement, analogue and digital parts faces each other and shielding is the only possible way to reduce coupling.

The goals of FE-TC4-DS Tier ([3], [4]) are first to verify that the Tier 1 is working correctly and second to study the parasitic coupling between Tiers. This Tier is composed of a matrix of pixels with the same dimensions as the analogue Tier 1. This digital pixel is sketched in Figure 6.

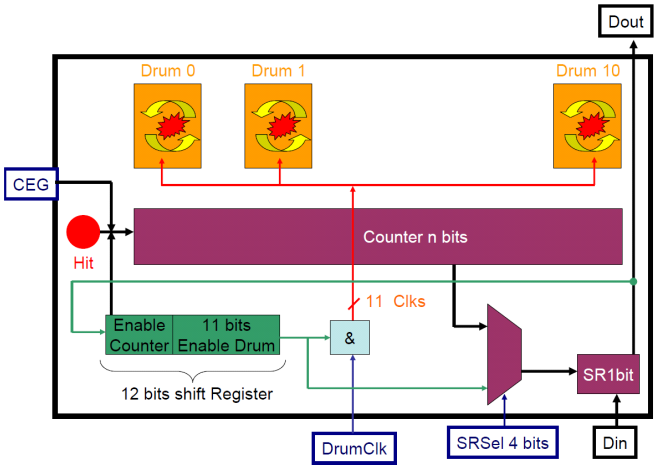

Figure 6: FE-TC4-DS pixel structure

"Hit" is the output of Tier 1. Signal called "CEG" (Count Enable Global signal) enables counting for all the pixels. Counting of a digital hit (for test) is also possible. A counter of 11 bits is used to count the number of hits. The result can be read via a 1-bit shift register.

To study the parasitic coupling between the two Tiers, the so-called "drum" cells are designed to generate digital noise in front of specific structures of the analogue Tier. Eleven different structures corresponding to specific analogue functions can be identified in the layout of the pixel, as shown in Figure 7.

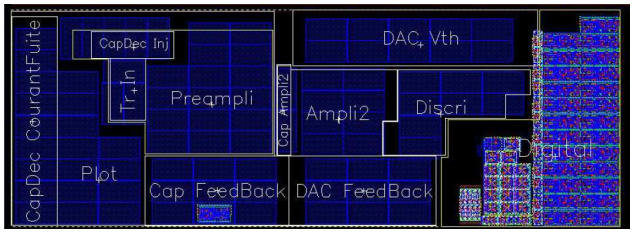

Figure 7: Analogue pixel layout: 11 specific areas

In front of each area, a drum cell has been designed with the structure described in Figure 8. The only function of these drum cells is to generate digital commutation (digital noise). An 11-bits shift register per pixel will configure these cells: Each drum cell can be activated (or not) independently of the others.

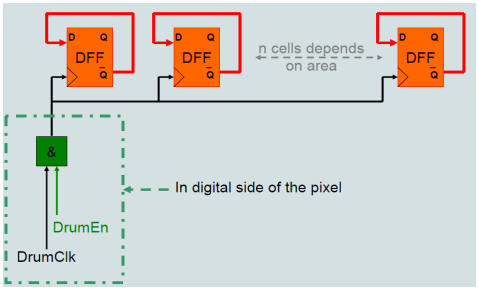

Figure 8: A “drum” cell

Moreover, in order to study a possible effect of shielding, different column layout configurations have been implemented. Five columns are designed without any shielding, 4 columns with shielding made of metal 5, 2 columns with shielding made of metal 3 and 2 columns with both shielding (metal 3 and metal 5).

B. *FE-TC4-DC : Complex read-out chip*

FE-TC4-DC is the second digital read-out Tier that will be bonded to the analogue Tier. For a design as realistic as possible with respect to the ATLAS pixel requirements, the architecture chosen is very similar to what the architecture of the future FE-I4 will be ([5], [6]). In particular, it is based on the same 4-pixel regional structure that will be sketched below. But due to time constraints, a simplified periphery and readout control logic was aimed for. After introducing the 4-pixel digital region, this periphery will be described underlining the main differences to the FE-I4 architecture.

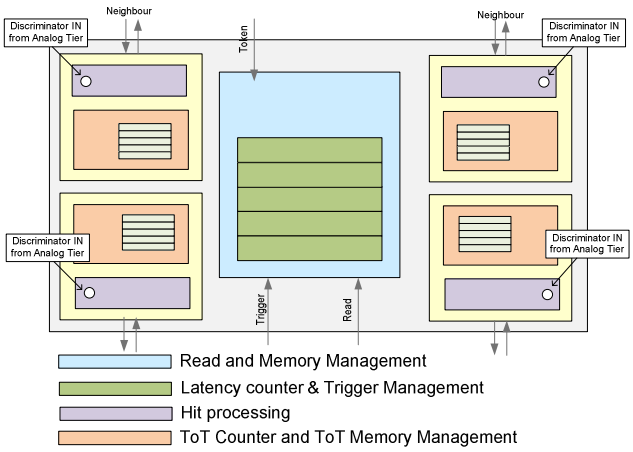

Figure 9: The 4-pixel regional digital logic

The 4-pixel architecture is schematized in Fig. 9. These four pixels form a 2 by 2 pixel block inside a Double-Column In this design, latency counters and trigger management units, as well as read and memory management units are shared between four adjacent pixels. The pixels still retain individual Time over Threshold (ToT) counters, as well as individual hit processing circuitry. Any discriminator that fires in the corresponding four analogue pixels starts the common latency counter in the digital Tier, effectively time-stamping a particular event. It is to be noted that when several pixels are hit in the same bunch-crossing inside a single 4-pixel region, a single latency counter is allocated. This has the important consequences of reducing digital activity, reducing digital power and improving the efficiency of the architecture. This structure is also well tuned to the physics, as real pixel hits come clustered. Furthermore, it is possible to distinguish in the digital logic small hits from big hits, by the time their comparator stays above threshold. The logic allows smaller hits to be associated with bigger hits in their immediate vicinity, either in the same region, or in adjacent regions (so-called “neighbor logic” mechanism). This provides a handle to avoid recording these small hits with time-walk. One difference at the 4-pixel region level with respect to the FE-I4 is the existence of a hit memory, which forms the basis of a column level readout shift register. This readout shift register provides an alternative way to read out pixel hits.

The complete Double-Column is made of 31 4-pixel regions, the top region having two dummy inputs as the corresponding analogue Tier contains only 61 pixels per column. To simplify the periphery, signals which are used in the FE-I4 full scale chip for the reading out of data and for the communication of the pixel hits to the periphery, related to the FE-I4 control block, need to be provided from the outside for this prototype. There is also an alternative way available to read-out data through a simple shift register. Finally, configuration of the chip and simple readout is achieved through multiplexed shift registers controlled through 2 enable bits.

V. Sensor Connection

In order to build a hybrid pixel detector, connections to a silicon sensor have to be done. We decided to keep the IZM bump-bonding technology already employed for ATLAS pixel modules (and foreseen for the upgrades).

Analogue and digital Tiers are bonded face to face. Only Tier 1 is thinned. Backside metallization on Tier 1 is used to form both wire-bond pads (for circuit inputs and outputs), and bump-bonding pads (above each pixel for sensor connection). Hence, due to geometric constraints, the sensor must be smaller than the read-out matrix. The sensor illustrated in Figure 10 is reduced to 7 columns of 48 pixels (instead of 14 columns of 61 pixels for Tier 1 matrix). The complete 3D final assembly is depicted in Figure 11.

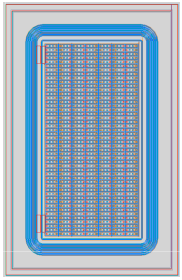

Figure 10: Sensor layout

The design of this sensor has been done by the Munich group (Max-Planck-Institut für Physik, Werner Heisenberg Institut).

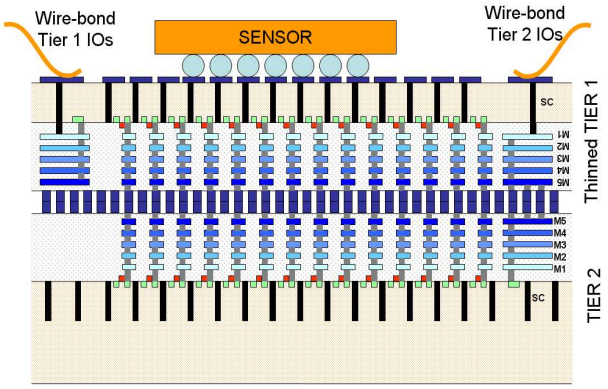

Figure 11: 3D final assembling for FE-TC4 project

VI. 3D TEST CIRCUITS

In each FE-TC4 sub-reticles test circuits have been implemented for testing Chartered technology and 3D basic elements. Test structures are grouped into four chips which will be bonded in 3D configuration at the same time as the other chips of the project.

- Evaluating capacitances:

Values of preamplifier feed-back capacitor and injection capacitor can be measured on dedicated arrays of 1024 capacitances. An array of 100x100 Super-Contacts is also implemented to measure the equivalent parasitic capacitance of one Super-Contact (relative to the substrate).

- Testing Super-Contact influence on transistors:

Super-Contacts are thin but deep vias which can be placed closed to transistors (minimum space with active region is 0.5µm). To evaluate influence of this new generation of contacts on transistors performances and to evaluate the involved parasitic coupling, different test structures have been designed. These test structures include enclosed and linear transistors placed at various distances from Super-Contacts. Moreover a signal can be applied on Super-Contacts in order to study the influence on transistors which have been implemented with different configurations of substrate tap ? or Nwell rings.

- Testing Bond Interface and Super-Contact connection reliability:

These tests can be performed only in 3D configuration. As depicted in Figure 12, chains of interface bonds connected in series with Metal 5 and chains of Super-Contacts are implemented to evaluate the rate of successful connections. The expected result of these tests is a very good yield as announced by Tezzaron.

- Testing the mechanical quality of thinned chip:

Creating Super-Contacts, bonding face to face the two Tiers, thinning Tier 1, and bonding on this thinned Tier may generate mechanical stresses, especially on Tier 1 areas where input-output pads are implemented. Test structures like linear PMOS, enclosed PMOS, feed-back capacitances array, injection capacitances array, poly-silicon resistance and shift registers are implemented under or closed to wire-bond pads (Back-Side metal).

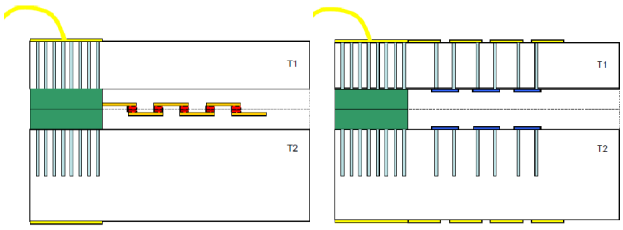

Figure 12: Tests structures for Bond Interface (left) and Super-Contacts (right) reliability

VII. FE-C4 PRELIMINARY TEST RESULTS

Porting directly one design (FE-I4-P1) from IBM 2D technology (8LM) into Chartered 3D technology (5LM) appeared to be quite challenging. In order to disentangle problems due to the technology itself from problems caused by 3D connections and stacking, we decided to make a first step consisting in a simple conversion from IBM to Chartered 2D (8LM). The resulting chip, called FE-C4-P1, is an exact translation of FE-I4-P1, and, due to a tight schedule, even the transistors sizes remain unchanged, leading to an un-optimized choice of their dimensions. No detailed simulations except the "typical" case have been performed.

Submission of this chip had been done in February 2009 and the chip has been tested in early May.

Preliminary results are very encouraging: Chip functionalities are fully working and analogue results (measured with the LBL set-up previously used for FE-I4-P1 tests) have demonstrated performances comparable to those of the IBM chip. Minimum matrix threshold close to 1000 e-, noise about 80 e- rms and threshold dispersion (un-tuned) of 200 e- have been measured.

One fundamental characteristic needed for IBL or SLHC upgrades is radiation tolerance up to few hundred MRad. SEU behaviour of the chip is also an issue. Irradiation of FE-C4-P1 has then been carried out using CERN_PS irradiations facility with 24 GeV proton beam up to about 400 MRad. After approximately 160 MRad, we noticed a problem on the digital registers of the chip which tend to stay "blocked" in the "1" state. These registers can only returned to the "0" state by power-off of the chip. We currently think that this effect is due to the shifts of P-Mos and N-Mos transistors' VTs caused by the irradiation of this non-optimal design which tends to encourage the "1" state.

This problem, which could be easily corrected in the next versions of the chip, gives in turn a problematic tuning of all the currents which drive the analogue parts. However, we were able to make analogue measurements of few tenths of pixels after 400 MRad. The mean noise of these set of pixels has been measured at 230 e- rms: Even if it is a factor 3 higher than the one measured before irradiation, it stays at a reasonable level. Thus no show-stopper concerning radiation hardness of Chartered technology has then been detected.

VIII. CONCLUSION

Benefits of 3D circuits appear evident: Pixel size can be decreased by separating digital function in another Tier. Alternatively, more functionalities can be implemented in front of each analogue pixel. Moreover, each Tier can be designed in a different technology for better performances.

This chip is one of the first chips demonstrating the feasibility of such 3D circuit. By the end of the year 2009, hopefully, tests results would confirm the functioning and the quality of the assembling and will reinforce the position of 3D architecture for future detectors technology selection.

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