Integrated test environment for a part of the LHCb calorimeter– TWEPP-09

C. Abellan [a], M. Roselló [a], A. Gaspar de Valenzuela [a], J. Riera-Baburés [a]
D. Gascón [b], E. Picatoste [b], A. Comerma [b], X.Vilasís-Cardona [a]

[a] LIFAELS, La Salle, Universitat Ramon Llull. Quatre Camins 2-4, 08022 Barcelona, Spain.
[b] Departament d'ECM, Universitat de Barcelona, Diagonal 647, 08028 Barcelona, Spain.

cabellan@cern.ch

Abstract

An integrated test environment for the data acquisition electronics of the Scintillator Pad Detector (SPD) from the calorimeter of the LHCb experiment is presented. It allows to test separately every single board or to perform global system tests, while being able to emulate every part of the system and debug it. This environment is foreseen to test the production of spare electronic boards and help the maintenance of the SPD electronics along the life of the detector. The heart of the system is an Altera Stratix II FPGA while the main board can be controlled over USB, Ethernet or WiFi.

I. Introduction

The maintenance of the electronics for the LHC experiments should be an issue along the life of the detectors. Electronic boards will have to be repaired or tested while the original designers and testers of the production electronics may not be anymore involved in the experiment. For this reason the need of self contained, easy to use and well documented test setups becomes almost mandatory.

The LHCb calorimeter is made of four chambers namely a hadronic calorimeter, an electromagnetic calorimeter, a preshower (PS) and Scintillator Pad Detector (SPD). The role of the SPD is determining whether the crossing particle is charged or neutral to complement the information from the preshower mainly for the trigger system.

In this paper we present the design and implementation of such a test bench setup for the SPD of the calorimeter of the LHCb experiment. [1]

In a first part, we will briefly describe the different electronic boards found at the SPD, describe their basic functions and the relationship between them.

In a second part, we will describe the former test boards, the ones used during prototyping and production testing. We will describe the tests these boards where capable of and some of their handicaps.

In a third part, we will describe the implemented solution and describe the improvements performed on the system.

Finally in a fourth part, we will take brief conclusions.

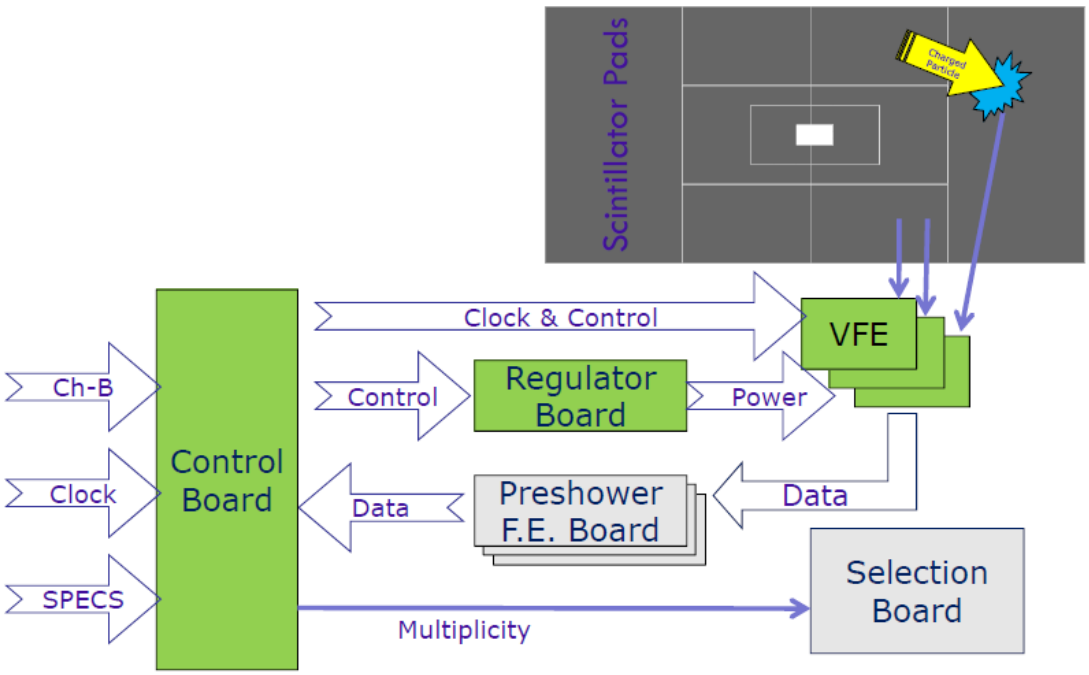

Figure 1: SPD simplified diagram

II.SPD Electronics

The SPD is formed by a plane of detecting cells made of plastic scintillator. These cells contain an optical fiber which transports the produced light to the corresponding input channel of a 64 channel multi-anode photomultiplier R7600-00-M64MOD from Hamamatsu (aka PMT).

For each PMT we have a Very Front End electronics card (VFE) which is in charge of performing the analogical signal processing and the digital conversion. This analogical signal processing mainly consists in integrating the signal, subtracting a fraction of the previous pulse to correct for spill over and, finally, comparing to a programmable threshold for each clock cycle. This process is sensitive to the starting integration time which is controlled by the edge of a clock signal sent through the so called control cables. Control cables also have a synchronous serial line for low latency operations such as test pattern start and stop. Every VFE sends the obtained digital information serialized by the so called Data Cable (DC) at a payload data rate of 2.6Gbps. VFE boards are powered by specific radiation tolerant regulator chips hosted in a Regulator Board (RB).

The connection of VFEs and RBs with the experiment control system as well as the clock distribution is made by Control Boards (CB). RBs use the same physical and electronic interface as VFEs so there is no difference from the CB's point of view.

The data obtained by VFEs is sent to the Preshower Front End Board (PSFEB) which are the boards in charge of processing the PS signal and sending the information to the trigger and data acquisition paths (DAQ).

CBs also contribute to the trigger system by collecting the SPD bits from a detector region and adding them up to evaluate its multiplicity. This calculation is made by adding the multiplicity coming from 4 or 7 VFEs sent by the corresponding PSFEBs. This yields to about 5.9Gbps of input data. The multiplicity is sent to the Selection Board (SB) by a dedicated optical fiber.

All these boards and their links are summarized on Figure 1 and further information can be found in [2]

III. Former Test Boards

A. FPGA Baseline

The data rates of this systems make necessary the use of FPGAs to implement the test boards. The original FPGA used for all test systems in our labs was a board by a vendor called Parallax[3] that included a Stratix EP1S25F672C6. The form factor of this board makes it appropriate for prototyping purposes as it can be used with relatively small footprint and a single power supply, the connectors are simple and inexpensive and easy to exchange.

Unfortunately this product was discontinued by the vendor so our group decided to make their own enhanced version. The original idea was to keep the board backwards compatible and add more pins and capabilities.

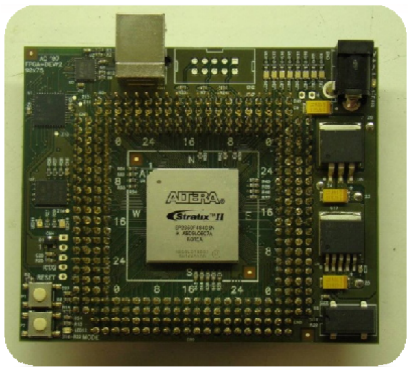

Figure 2: New FPGA board

The new board has practically the double of pins, a USB connection instead of the original serial one and a much more powerful Stratix II EP2S60F484C5. (a photograph can be seen in Figure 2)

B. Control Board Test

The CB was originally tested with a specifically designed board that emulated the backplane on which the CB is plugged. The original board can be seen in Figure 3.

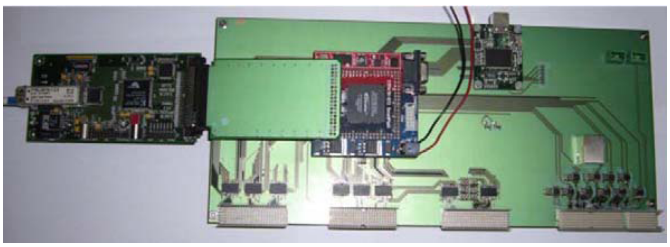

Figure 3: Former Test Board for CB

The test board communicated with a PC by a USB connection and also by a Serial Protocol for the Experiment Control System (SPECS) which is an *ad hoc* protocol. [4]

The FPGA was also connected to an *ad hoc* optical receiver [5] that could monitor data going out from the CB.

Let us note that this setup needed two power supplies and a precision clock generator to work properly. Besides, the physical robustness was an issue.

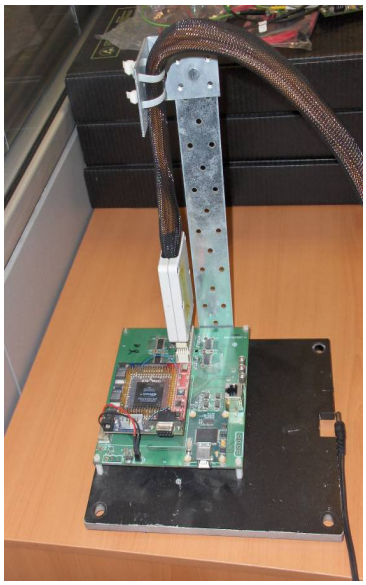

Figure 4: Former Test Board for VFE

C. Very Front End Test

VFEs are more complex to test since they have an optical and a digital part.

The digital part is tested with a board that emulates the roles of the CB and PSFEB. This board has also connectors to interface with the optical testing part. In this way, the digital test system can trigger a pulse of light and receive the obtained data from the VFE, everything with accurately controlled timing. A photograph can be seen in Figure 4.

The analogical part is tested in a separated test bench designed to pulse light into the PMT as seen on Figure 5. This requires a high voltage power supply, a dark box, and a motorized optical fiber that illuminates only the desired pixel of the photomultiplier.

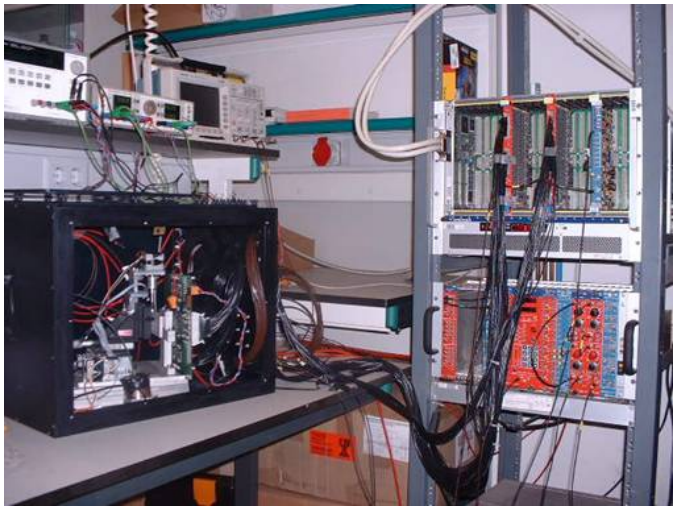

Figure 5: Analogical Test Bench for VFE

D. Link Test

There were also some other small boards designed to supervise links between different parts of the electronics. For example clock distribution was very important and a board was designed to supervise not only the timing but also the shape of the differential signal in both sides of the cables. A photograph of the board can be seen in Figure 6.

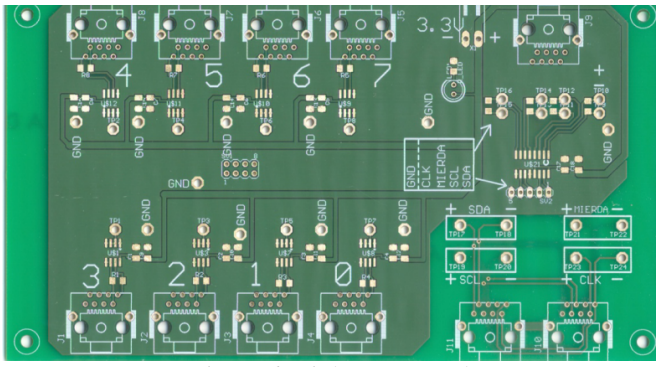

Figure 6: Link Test Board

E. Mixing Detector and Test Boards

Test boards were used not only during production verification and debugging of the electronics but also to check its correct installation.

These tests showed the usefulness of connecting the electronics to test boards but also to connect a part of the electronics to the final detector environment. This is not only interesting because of the ability to isolate errors but also because during installation not all the other parts need to be installed to test the current one.

As an example we could test the VFEs when the PSFEB were not installed yet. We used the CB to control the VFEs but a test board to receive and check incoming data.

IV. Integrated Test Environment

The integrated test environment solves all the problematic aspects we have found by using the former test environments and adds all the small enhancements that simplify the testing process.

Some examples are the extensive use of serigraphy on the board to ease its use and avoid having to look for information elsewhere. Another example is having a mechanically robust environment.

Another interesting feature is to have a self contained test environment requiring a minimal laboratory setup. The new board regulates its own voltage, so it is possible to operate with a single power supply like the one used in laptops. This makes the system more compact and less error prone with respect to the input voltage.

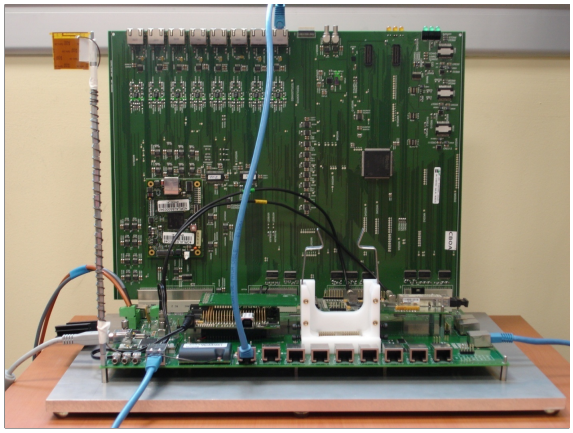

Figure 7: Integrated Test Environment for the SPD

A. Test Capabilities

The new test board integrates all the testing capabilities that former boards have. This includes testing all parts from the CB, that are:

- Data from the VFEs to CB through PSFEBs
- Data going out of the CB by the optical link
- Control performed by the CB

- Precise clock distribution
- SPECS bus communication
- Interaction with other parts of the experiment

It also has the capabilities of the digital VFE test board, that are:

- Receiving data from a VFE
- Controlling a VFE as a CB would do
- Controlling a RB as a CB would do
- Triggering the optical test environment

And finally it is able to do all the things a Link test board was able to do:

- Inspecting communication CB ↔ VFE
- Inspecting delays between clocks in a CB
- Acting as a passive VFE with terminated input

B. Connectivity

The new test environment is able to connect separately with every board as also were the preceding test boards performing the same tests on them. But it is also able to connect to all of them at the same time being able to transfer data from one test to the other one. (Figure 8)

It could be argued that with the preceding test boards, it could have been possible to connect various boards to a single PC and by software means transfer data from one controlling software to the other controlling software and this way "close the loop" of data flow. The reality is that data transmission speeds were far too low to do this kind of links, with just a couple of Mbps when it would have required thousands of Mbps.

In the new board all data flows from/to the FPGA, so all links are made inside it.

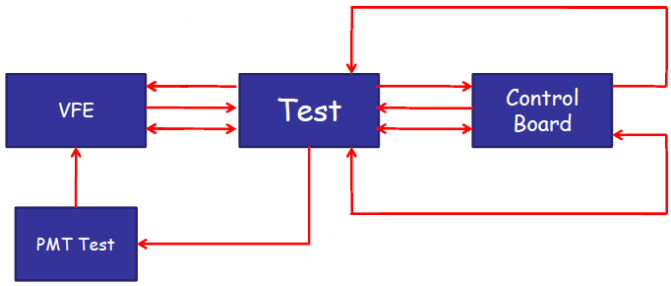

Figure 8: Connection Diagram 1

Another interesting option is controlling a VFE through a CB controlled by the test board, this way it is possible to inspect the behaviour of the system acting mounted in the exact way it would be in the real detector. (Figure 9)

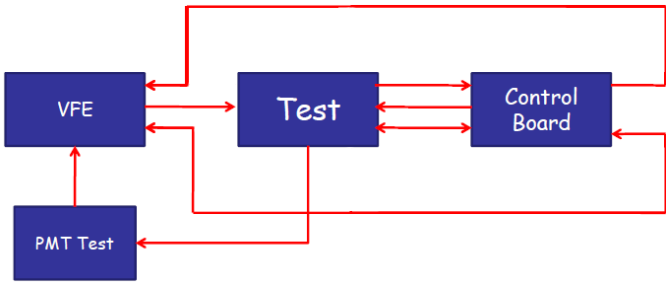

Figure 9: Connection Diagram 2

C. Additional Features

Further improvements have been made to the system such as a new interface that supports Ethernet and/or WiFi connections. This implies a different approach to the problem of interaction between the board and the controlling PC. Instead of running software in the PC that handles the board as an instrument to retrieve data, the idea is that the board runs all the necessary software and the PC is only an interface to the user.

Having this interface has some advantages such as being Operative System independent – because the PC only accesses to a web server embedded in the board – and not requiring the PC to have any software with the problems it implies, like having different computers and keeping them with an updated software.

Another advantage is that by using this kind of interface it is possible to use the boards remotely. For example, an expert could manipulate the board under test from his homeland university. Another option would be leaving the test board in the experimental zone connected to the local network and handle it from the control room.

Figure 10: Xport Ethernet Interface

It all is easy to do because of the use of a commercially available web servers that include all necessary electronics and are interfaced by a serial line [6] (Figure 10).

Another improvement is having a much more mechanically resistant structure. A 10mm thick aluminium plate has been used together with 21 fixation screws to give both strength and stability to the whole board (see Figure 11). The plate is also used to dissipate the heat produced by the inboard regulator.

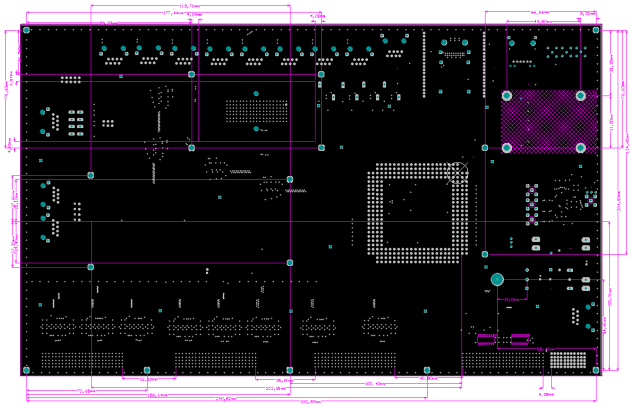

Figure 11: Mechanical Drawing of the Integrated Test Environment

Some more improvements have been made in the mechanical design like good fixation for the big LVDS connectors from data cabling or better fixation of the optical receiver board.

The usability has been another aspect taken into account, and thinking that future tests will probably not be used in a fully equiped laboratory, the board has been made as independent as possible. For example now the board has an embedded clock generator capable of generating its own clock – both at the exact frequency of the experiment or with small deviations – , but also capable of receiving an external one and filter it to reduce the possible jitter. Another example already mentioned is the use of a single power supply.

These are small improvements but have a large impact on the test procedure.

V. Conclusions

As mentioned in the introduction, the main aim of the work done was to be ready for future reparations and maintenance of the different electronic boards of the LHCb SPD. The whole design was from the beginning intended for an average user, not only experts. This implies the system to be usable, stable, less lab dependant and eventually remotely operable by an expert.

This was possible because of the use of a better interface that includes net capabilities.

We have solved the problems that we have discovered during the real use of all the previous test systems.

And finally some more test possibilities have been added to be able to test more complex scenarios in prevision of future complex problems.

VI. Acknowledgements

This work is partially supported by the Spanish MEC (project FPA-2008-06271) and by the "Generalitat de Catalunya" (AGAUR 2005SGR00385).

C.A.B. Would like to thank the "Generalitat de Catalunya" for an F.I. Grant.

VII. References

[1] The LHCb Collaboration, A.Augusto Alves Jr. et al. *The LHCb detector at the LHC* Journal of Instrumentation Volume 3, S08005 (2008).

[2] D.Gascón et al, *The Front End Electronics of the Scintillator Pad Detector of LHCb Calorimeter*,12th Workshop on Electronics For LHC and Future Experiments, Valencia, Spain, 25 - 29 Sep 2006, pp.153-157

[3] http://www.parallax.com/

[4] Breton, D; Charlet, D, *SPECS: the Serial Protocol for the Experiment Control System of LHCb,* LHCb public note*:* CERN-LHCb-2003-004

[5] Lax, Ignazio ; Avoni, G ; D'Antone, I ; Marconi, U, *The Gigabit Optical Transmitters for the LHCb Calorimeters,12th Workshop on Electronics For LHC and Future Experiments, Valencia, Spain, 25 - 29 Sep 2006, pp.153-157*

[6] http://www.lantronix.com/