Gossipo-3: A prototype of a Front-End Pixel Chip for Read-Out of Micro-Pattern Gas Detectors

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Abstract

In a joint effort of Nikhef (Amsterdam) and the University of Bonn, the Gossipo-3 integrated circuit (IC) has been developed. This circuit is a prototype of a chip dedicated for read-out of various types of position sensitive Micro-Pattern Gas detectors (MPGD).

The Gossipo-3 is defined as a set of building blocks to be used in a future highly granulated (60 μm) chip. The pixel circuit can operate in two modes. In Time mode every readout pixel measures the hit arrival time and the charge deposit. For this purpose it has been equipped with a high resolution TDC (1.7 ns) covering dynamic range up to 102 μs. Charge collected by the pixel will be measured using Time-over-Threshold method in the range from 400 e⁻ to 28000 e⁻ with accuracy of 200 e⁻ (standard deviation). In Counting mode every pixel operates as a 24-bit counter, counting the number of incoming hits.

The circuit is also optimized to operate at low power consumption (100 mW/cm^2) that is required to avoid the need for massive power transport and cooling systems inside the construction of the detector.

I. Introduction

A number of features make Micro-Pattern Gas Detectors [1] (MPGD) attractive to be used in particle-physics experiments, astro-particle research and medical imaging. Among those are high spatial resolution, radiation hardness and inherent low material budget. The availability of highly integrated readout electronics allows for the design of gas-detector systems with channel densities comparable to that of modern silicon detectors. Main specifications of such an IC will be compatible with requirements imposed upon the ATLAS Pixel System for Upgraded Luminosities.

In 2007 we submitted the Gossipo-2 chip [2] as a prototype of a pixel readout array featuring high resolution TDC-per-pixel architecture. Although this design was successful, it has been found that some blocks of the circuit need modifications.

The main goal of the present prototype called Gossipo-3 is to optimize the design of the building blocks for a future IC dedicated for readout of MPGD's (e.g. the Timepix2 chip). .

II. Micro-Pattern Gas Detectors

A Micro-Pattern Gas Detector (see Figure 1) is position-sensitive proportional counter. A gas layer is used as signal generator. Construction of the detector includes a CMOS pixel array and a Micromegas placed at the distance of 50 μm on top of it by using a wafer post-processing technology (Integrated Grid or InGrid) [3], [4]. Above this grid a cathode foil is built. The cathode foil and the grid are put at negative voltage and the pixel array surface is at ground potential. The volume between the drift foil and the pixel array is filled with a suitable gas mixture.

When a minimum ionizing (MIP) particle passes the drift gap (see Figure1), some primary electron-ion pairs will be created along the track. Driven by an electric field, primary electrons will drift towards the pixels [5]. In the InGrid-pixel gap an avalanche multiplication occurs making the charge sufficient to activate an on-pixel integrated circuit. The activated pixels will give the complete image of the track (projection of the track on the array surface). Moreover the drift time measurements at the activated pixels will indicate the vertical coordinates of the primary electrons. By combining the data of all participating electrons, a track segment can be reconstructed in space.

A point of concern are high voltage breakdowns (discharges) occurring in the InGrid-pixel gap. These can damage or destroy the read-out chip. This problem has been solved by placing an adequate protection layer on the surface of the chip. In this case the charge of the discharge is limited by the capacitance of the protection layer attributed to the pixel and is only 8 pC [6].
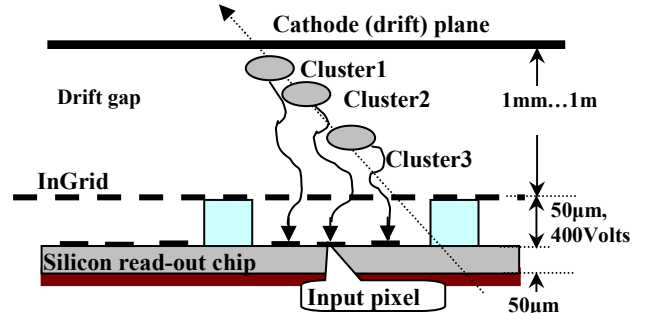

Figure 1: Layout of the micro-pattern gas detector with the amplification structure based on an integrated grid

The pixel readout chip is the basic component of the detector. It has to have a high densely pixel structure for accurate coordinate measurements. It should be able to provide high efficiency of detecting of single primary electrons. It is required to equip every pixel with a high resolution TDC for the drift time measurements.

III. The Pixel.

Each pixel in the Gossipo-3 prototype has a charge sensitive preamplifier and a discriminator to generate a Hit signal when the threshold level has been reached (see Figure2).
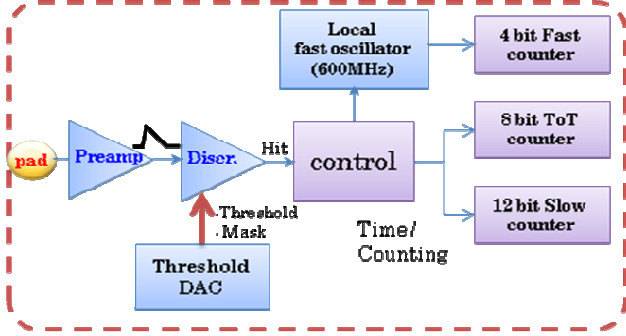

Figure 2: Block diagram of one pixel

In Time mode the digital part consists of a Local Oscillator, Fast counter, Slow counter and Time-over-Threshold counter. The Hit signal starts the data taking phase (see Figure 3). It triggers the Local Oscillator (LO) which starts to run at 580 MHz (T=1.7 ns) and activates Fast, Slow and Time-over-Threshold (ToT) counters. The LO will be stopped by the next rising edge of the external Clock signal (40 MHz). The Fast counter counts the number of signals at the output of the LO. In this way the delay of the Hit signal within one Clock period can be digitized. The Slow counter gives the number of full Clock periods (40MHz) in the time interval between the Hit and the Trigger signal. The final states of Fast and Slow counters present time position of the Hit signal in respect of the Trigger signal. The accuracy of the time measurement is determined by period of oscillation of the LO (1.7 ns). Both the period of the Clock signal (25 ns) and the number of bits in Slow counter (12 bits) determine the dynamic range (102 μs) of the measurement.

The ToT counter counts the number of full Clock periods (T=25 ns) in the time interval when the Hit signal is high. This time interval is proportional to the charge collected by the pixel. In this way the charge deposit can be digitized. The accuracy of the ToT method is limited by the noise-related time jitter on the non-steep falling edge of the signal (see Figure 3) at the output of the preamplifier (σ=27 ns corresponds to 200 e⁻). The ToT is linear proportional to the input charge in the range from 0 ns to 3 μs (corresponds to 28000 e⁻). This corresponds with the number of bits in ToT counter (8 bits) resulting in a 6.4 μs dynamic range ($25ns \bullet 2^8$).

With the arrival of the Token signal the data read-out phase is started. In this phase all the counters are configured into serially-connected shift registers. Driven by the Clock (40 MHz), the data will be shifted to the periphery of the chip. After the readout is completed all the counters will be reset.

In Counting mode the counters are combined into a 24-bit counter. In this mode only the information on the number of hits coming to the pixel in time interval between the Reset and the Trigger signals is available.

For the purpose of reducing dispersion of the threshold levels between the pixels, each pixel has a 4-bit DAC .
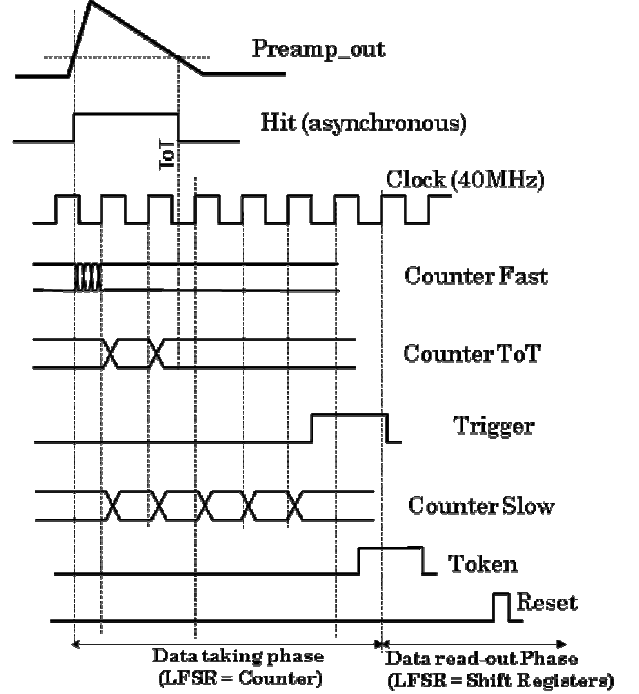

Figure 3: Time diagrams of operation in Time mode

IV. Front-end circuit.

In gas-filled pixel detectors parasitic capacitance at the input of the read-out circuit is very low (Cpar ≈ 10 fF). There is no need to compensate for the detector leakage current. This allows us design a compact, low-noise, fast, low-power front-end circuit optimized for high performance time measurements.

Besides a preamplifier, the circuit (see Figure 4) also includes a special device protecting the input against micro-discharges in the detector (see Chapter VI). The charge sensitive preamplifier has constant current feedback. In this topology the feedback transistor (Tfb) operates as a floating current source. The signal charge is integrated on the drain capacitance of the transistor which can be seen as a feedback capacitance in this topology. The capacitance has been chosen as small as 1 fF in order to provide high gain. The floating current source gradually discharges the feedback capacitance resulting in linear falling edge of the output signal. When no signal is present the feedback transistor operates as a 30 MOhm resistor.

In this circuit, the discriminator is capacitive coupled to the preamplifier. A constant current circuit controls the bias voltage at the discriminator input. It also provides recovery to the baseline after the hit. The time constant of the recovery has been chosen large (tens of microseconds) in order to avoid signal distortion. Channel-to-channel threshold dispersion is not influenced by the offset of the preamplifier and is determined by the mismatch in the discriminator circuit

(σ=70e⁻). With the help of the on-pixel DAC (4 bits) it can be reduced down to σ=5 e⁻.
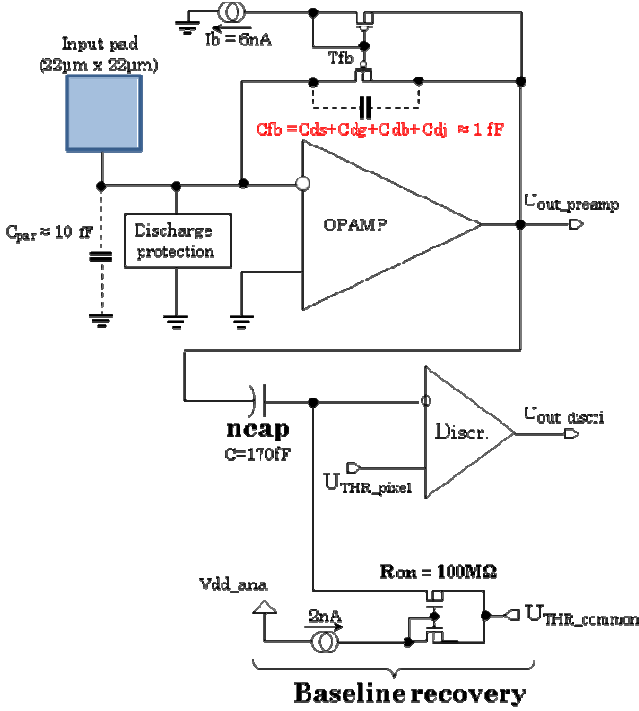

Figure 4: The front-end circuit

Even when having a power consumption of a few microwatts only, the front-end circuit demonstrates fast response (20 ns) and low noise (σ=70 e⁻).

V. Local oscillator circuit

The local oscillator circuit includes a NAND gate with a chain of inverters in the feedback (see Figure 5). A positive signal at the input triggers the circuit to oscillate at the frequency determined by the delay in the feedback. The oscillation frequency (580 MHz) is 14.5 times higher than the clock frequency (40 MHz). This means that 14.5 oscillator cycles are within one clock period and that the position of the leading edge of the input pulse can be determined with an accuracy of 1.7 ns.
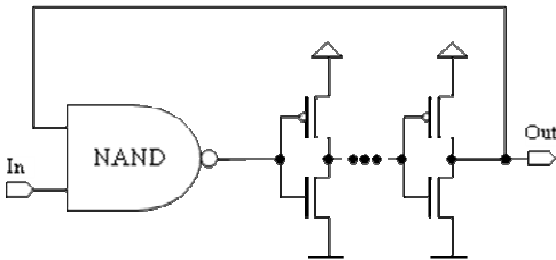

Figure 5. The local oscillator circuit

The gate delay of the CMOS inverters is sensitive to variations in the temperature and power supply voltage. Careful studies of the stability of the oscillator frequency show that the period of the oscillations is directly proportional to the temperature, with a slope of 2% per 10ºC, and inversely

proportional to the power supply voltage, with the slope of -12% per 100 mV. This is in agreement with simulations.

Modeling and measurements demonstrate that channel-to-channel spread of the oscillation frequency could be kept low, when the delay components are properly sized. Then even in the worst case (when the circuit is active within the whole clock period 25 ns), the accumulated error will be less than the period of oscillations (1.7 ns). This means that there will be no discrepancy on the number of pulses generated by different local oscillator circuits within one pixel array.

On the contrary, effects caused by variation of the fabrication process are much more significant. According to simulations the oscillation frequency in the fast corner is twice that in the slow corner.

Notice that the frequency could be set to the required value by adjusting of the supply voltage (Vdd) on the circuit.

In the fast corner, Vdd should be lowered and in the slow corner a higher value of Vdd is needed. In order to be able to tune the oscillator frequency a low drop voltage regulator (LDO) has been designed.

V. Low-drop voltage regulator

Figure 6 shows simplified schematic of the voltage regulator generating stable and adjustable (controlled by Uref) power supply voltage for all local oscillator circuits in the pixel read-out array. This topology involves an off-chip capacitor (10 µF). In order to reach required performance the capacitor has to have low equivalent serial resistance (less than 1 Ohm), on top of that the coupling to the capacitor (on-chip wiring and package bonding wires) needs to be low resistive.
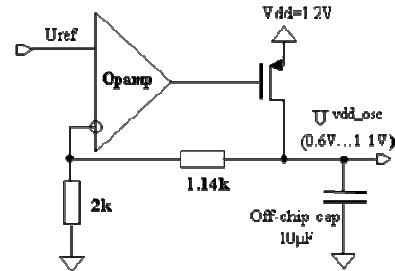

Figure 6. Simplified schematic of the LDO for all local oscillator circuits

The output voltage can be set in the range from 0.6 V to 1.1 V that is sufficient to adjust the oscillator circuits fabricated in all corners of the process. The circuit has a high PSRR (40 dB) in wide frequency range. The equivalent output impedance is low (less than 1 Ohm) and that allows to keep the output voltage stable when the load current changes.

VI. Discharge protection device

With the protection layer placed on the surface of the read-out chip the size of the discharge (in the case of high-voltage breakdown between the InGrid the pixel) is reduced down to 8 pC. And yet such a signal builds-up critical voltage at the input of the preamplifier and can damage the front-end circuit.

In the Gossipo-3 we use a standard N-channel transistor as a protection device (see Figure 7).
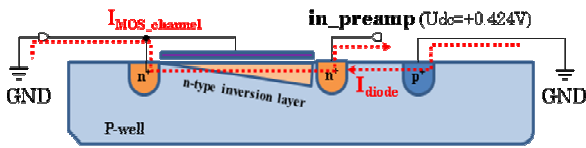

Figure 7. Layout of the device, protecting against discharges in the detector

In this device the drain, the bulk and the gate are tied to the ground and the source is connected to the node to be protected. The inversion layer under the gate and the p-n junction in the substrate form two channels draining the discharge current. So the voltage at the protected node will not exceed the critical level even when a small-size device (W/L=1μm/0.24μm) is used. Under typical operating condition this device does not introduce noticeable leakage current (250 pA) or parasitic capacitance (1.3 fF) into the circuit.

VII. Summary

The Gossipo-3 is a prototype of building blocks to be used in a future front-end pixel chip for read-out of Micro-Pattern Gas Detectors.

Every pixel will be equipped with a high resolution TDC (1.7 ns) covering a dynamic range up to 100 μs and a Time-over-Threshold counter to evaluate the charge deposit. The chip will also be able to operate in hit counting mode.

Each pixel has a low noise (σ=70 e$^-$), fast (response 20 ns) and low power (3 μW) front-end circuit optimized for high performance time measurements. A compact device is placed at the input of the front-end circuit providing protection against micro-discharges taking place in the detector.

For the purpose to tune oscillation frequency of the on-pixel local oscillator circuit a voltage regulator has been designed. It will provide stable, adjustable and load current independent power supply voltage for all pixel oscillators in the read-out array.

Gossipo-3 has been taped-out for MPW production run in 0.13 μm CMOS technology (September 2009).

VI. References.

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