FE-I4

-The New ATLAS Pixel Chip for Upgraded LHC Luminosities-

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(for the FE-I4 Collaboration)

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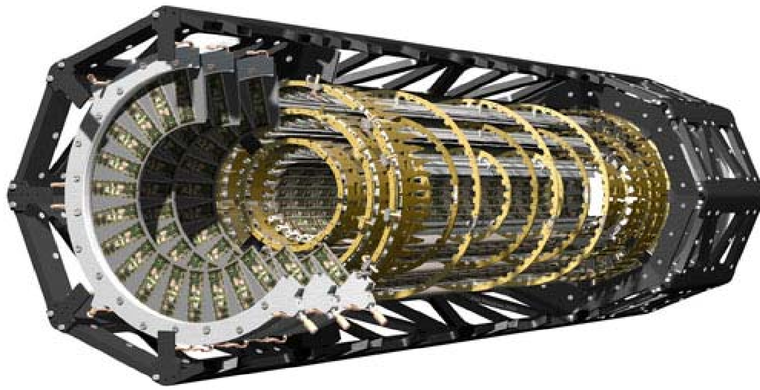
SI LAB
Silizium Labor Bonn

ATLAS Pixel Detector Collaboration

Contents

FE-I4 for IBL & sLHC

Present beam pipe & B-Layer

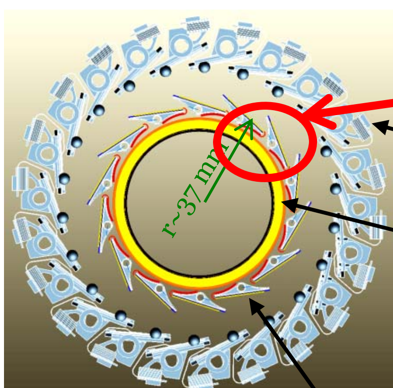


ATLAS Pixel Detector

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm

- IBL (~2014): inserted layer in current pixel detector.

FE-I4



Existing B-layer

New beam pipe

IBL mounted on beam pipe

- sLHC tentative layout (>2017): 4-5 pixel layers, small radii / large(r) radii (note: Discussion on boundary pixel / short strips, …).

- All Silicon.
- Long Strips/ Short Strips / Pixels.
- Pixels:
  - 2 or 3 fixed layers at 'large' radii (large area at 16 / 20 / 25 cms?)
  - 2 removable layers at 'small' radii

Motivation for Redesign of FE

- Need for a new FE? ⟶ FE-I3→FE-I4
  - Accommodate higher hit rate (smaller b-layer radius + luminosity increase) → Architecture based on local memories (no column-drain mechanism).
  - Smaller pixel size: enhanced granularity and reduced cross-section.
  - Reduced periphery & bigger chip: higher active area fraction (<75% → ~90%); cost down for sLHC (main driver is flip-chip, costs per chip).

    Big chip a challenge: power (routing, start-up), clk. distrib., yield…
  - Simple module: No Module Controller → More digital functions into the FE.
  - Power efficient design & new concepts: Analog design for reduced currents; decrease of digital activity (digital logic sharing for neighbor pixels); new powering concepts. 8 metal layers [2 thick Alu.] → Power routing.

- New technology: ⟶ 0.25 μm→130 nm
  - Higher integration density for digital circuits, radiation-hardness (no Enclosed Layout Transistor), availability on timescales of our experiments.

Some Target Specs for FE-I4

- Rad.-hardness: >200 MRad ionizing dose (FE-I3: >50 Mrad).
  Minimal guidelines: no ELT, minimal size and guard rings only for analog & sensitive digital circuitry.
- ToT coded 4 bits.
- DC leakage current tolerant to > 100 nA.

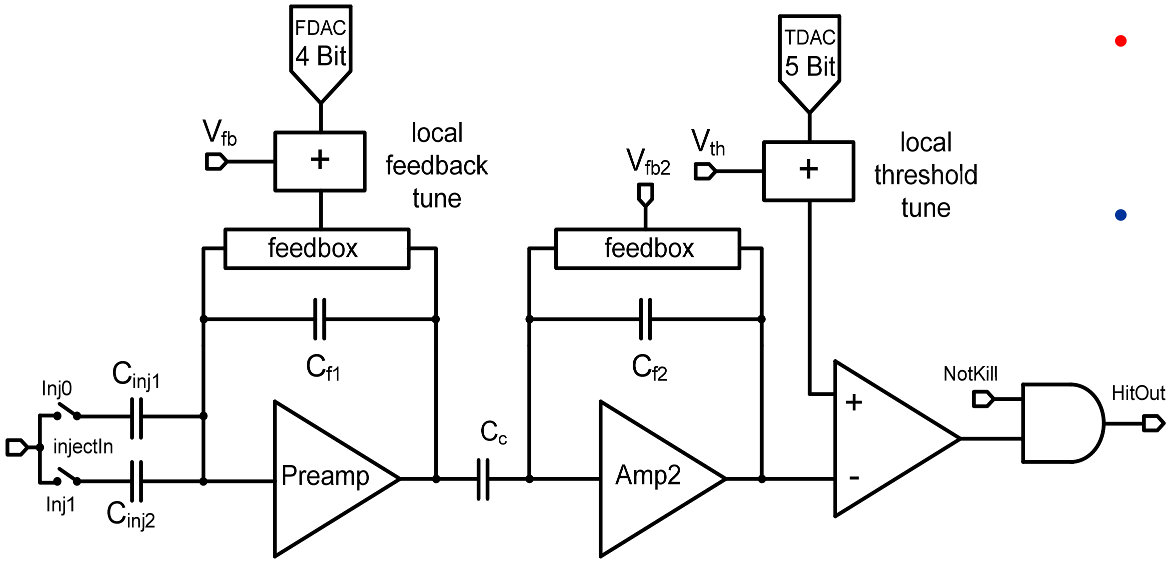
	FE-I3	FE-I4
Pixel Size [μm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Analog Current [μA/pix]	26	10
Digital Current [μA/pix]	17	10
Analog Voltage [V]	1.6	1.5
Digital Voltage [V]	2	1.2
pseudo-LVDS out [Mb/s]	40	160

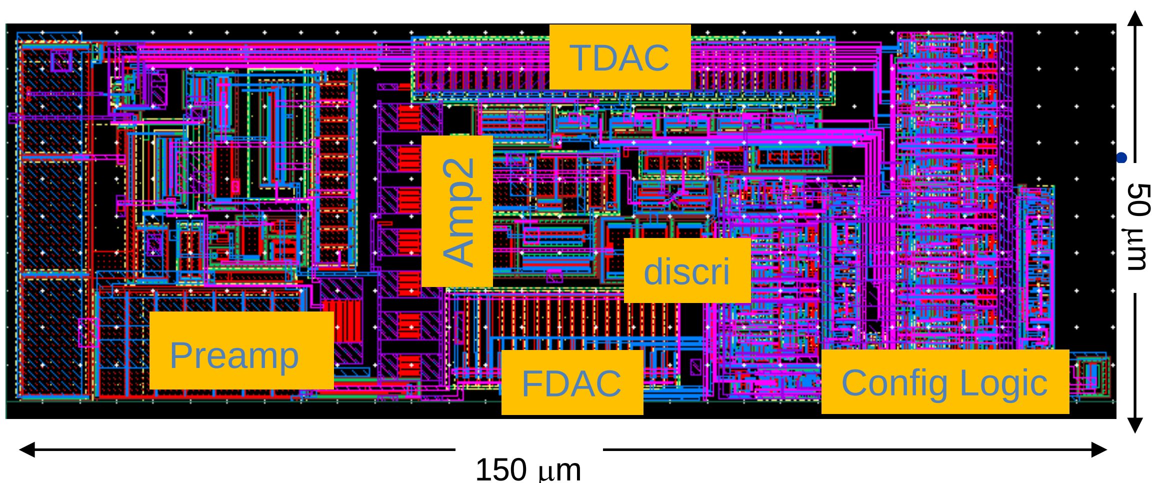
biggest in HEP to date

analog / digital power

tuned for IBL occupancy

Analog Pixel





- In FE-I4_proto1 (FE-I4 prototype submitted in 2008):

- 2-stage architecture optimized for low power, low noise, fast rise time.

→ regul. casc. preamp. nmos input.

→ folded casc. 2nd stage pmos input.

→ Additional gain, Cc/Cf2~6.

→ 2nd stage decoupled from leakage related DC potential shift.

→ Cf1~17fF (~4 MIPs dyn. range).

- 12b configuration:

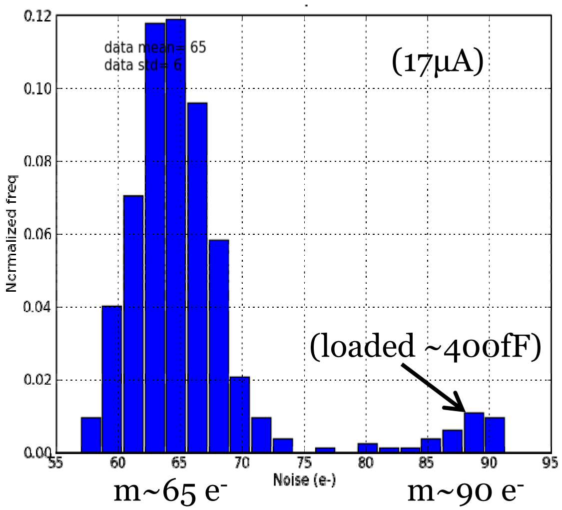
→ FDAC: tuning feedback current.

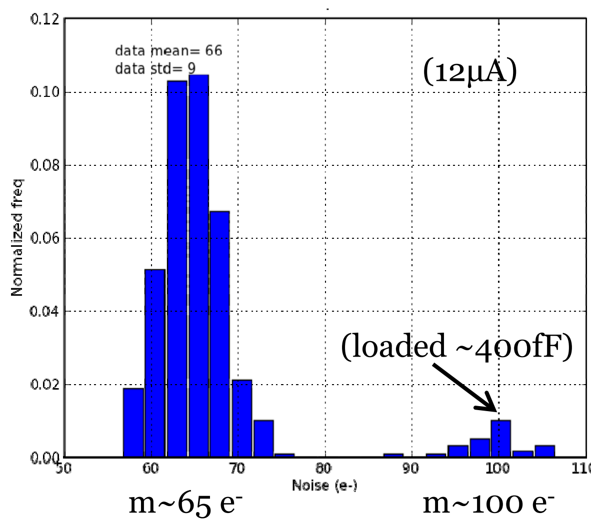
→ TDAC: tuning of discriminator threshold.

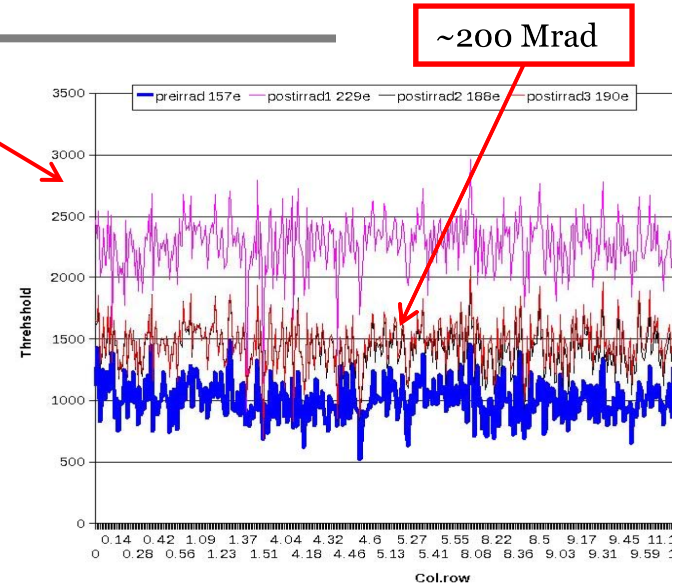
→ Local charge injection circuitry.

Analog Pixel: Noise & Irradiation

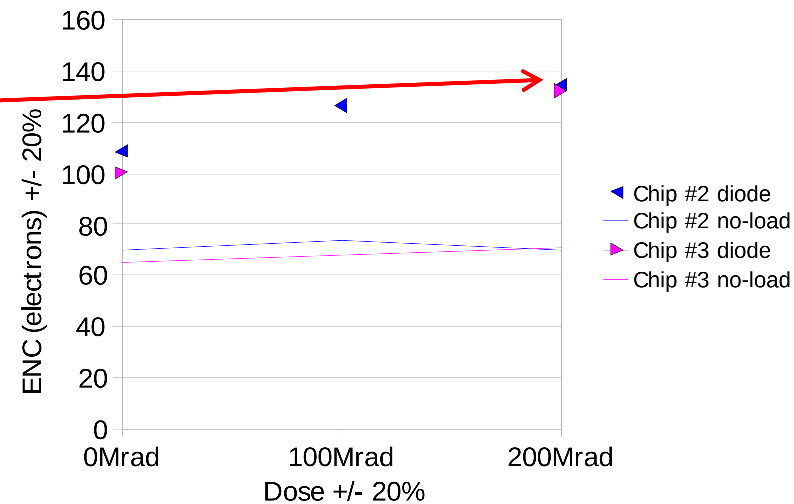
- Excellent un-tuned threshold dispersion.







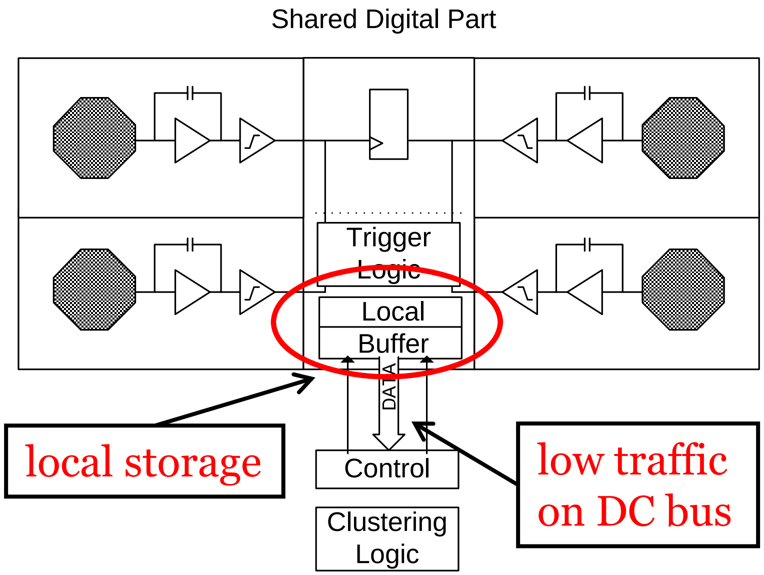
- Dose received: ~200 Mrad →
  Low I (10 µA): noise increases ~20 %.



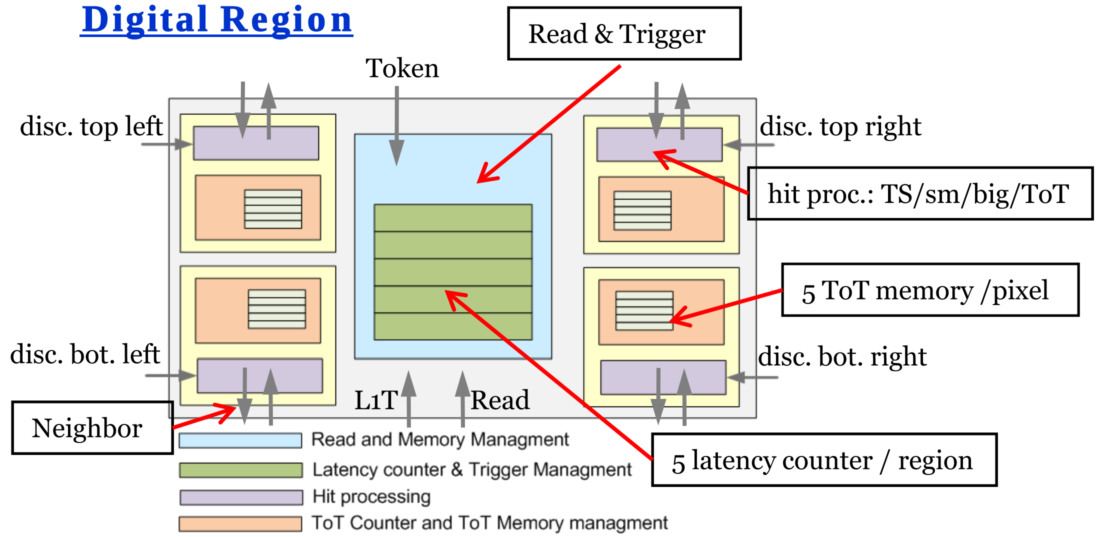
Low current (which is target value) is 10 µA/pixel
for preamp+amp2+comparator
Current for minimum noise: 17 µA/pixel

Digital Pixel: Regional Architecture

4-Pixel Unit



Digital Region



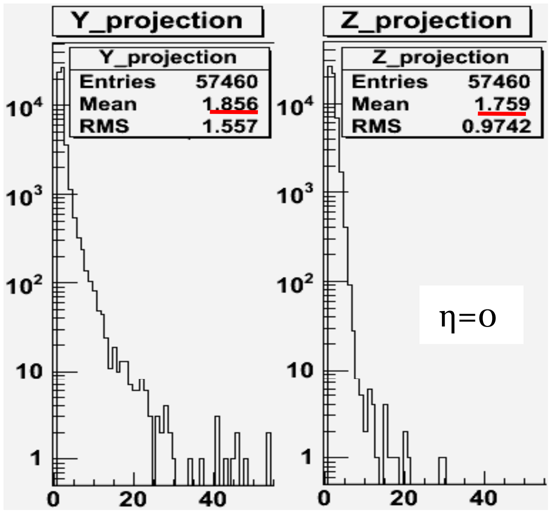
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Consequences:

- Spatial association of digital hit to recover lower analog performance.
- Lowers digital power consumption (below 10 µW / pixel at IBL occupancy).
- Physics simulation → Efficient architecture.

Performance / Efficiency

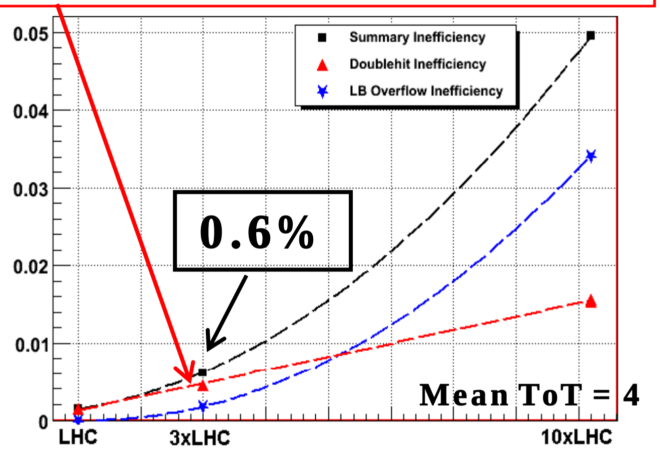
IBL: charge sharing in Z comparable to phi



Regional Buffer Overflow

Memories	Simulation		Analytical	
	IBL	10xLHC	IBL	10xLHC
5	0.047%	2.19%	0.029%	2.25%
6	0.011%	0.65%	0.003%	0.57%
7	<0.01%	0.16%	<0.01%	0.13%

@ IBL rate, pile-up inefficiency is the dominant source of inefficiency

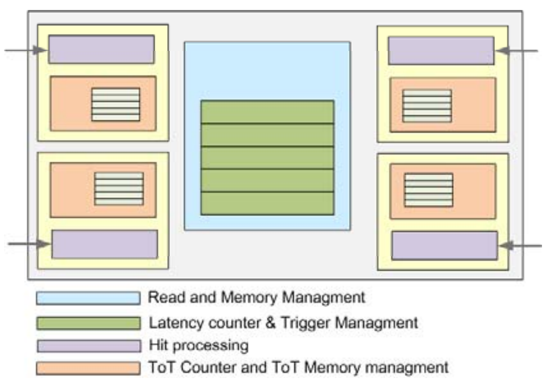


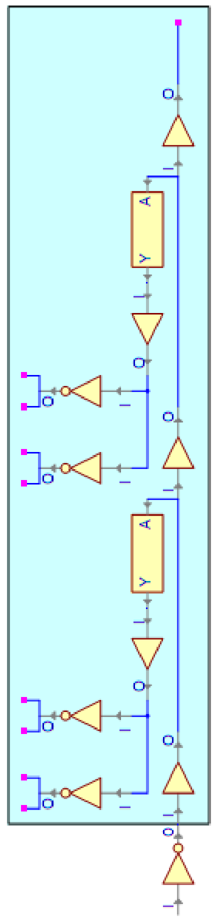
Inefficiency:

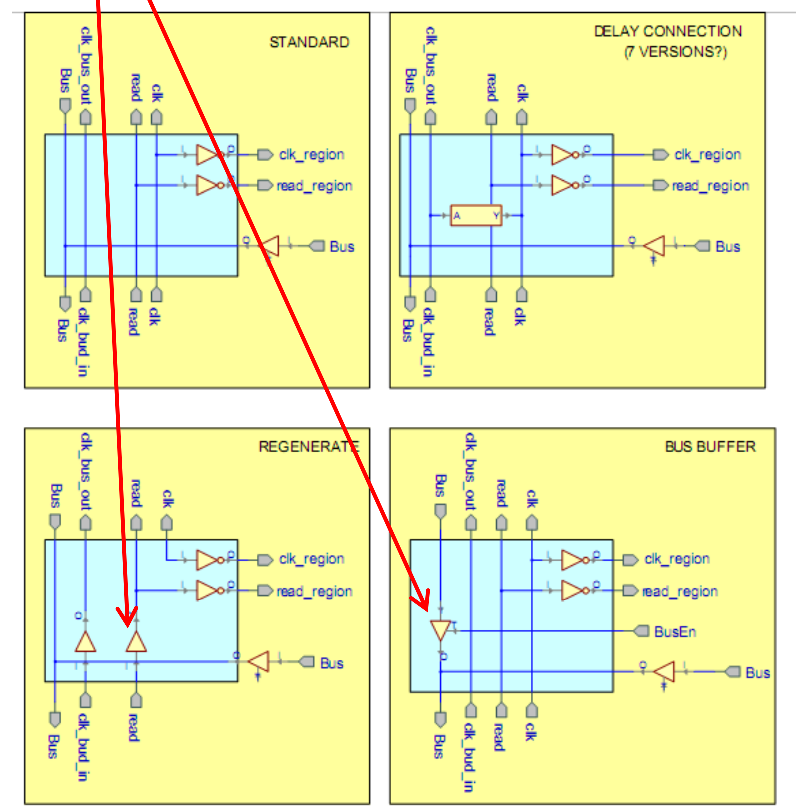
- Pile-up inefficiency (related to pixel x-section and return to baseline behavior of analog pixel) → ~ 0.5%.
- Regional buffer overflow → ~0.05%.
- Inefficiency under control for IBL occupancy.

Digital Column Architecture

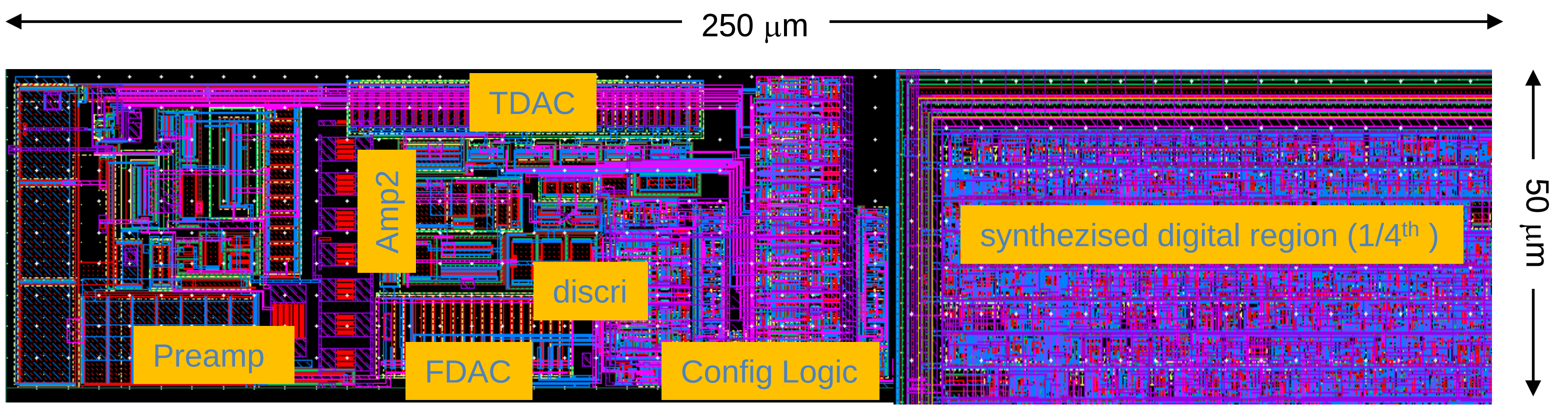
- 168 regions + CLK + buffering scheme → 1 digital DC

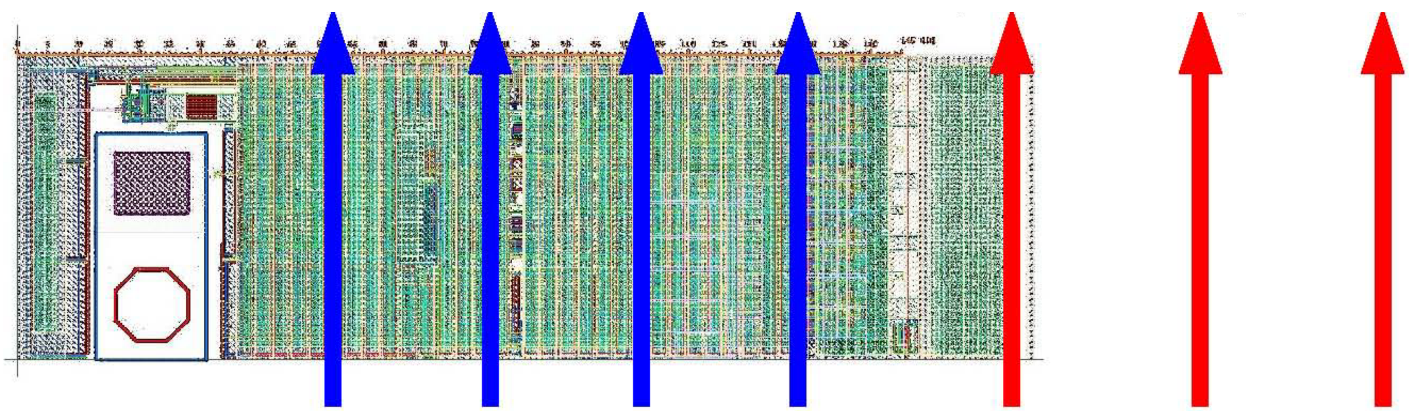






Pixel Layout

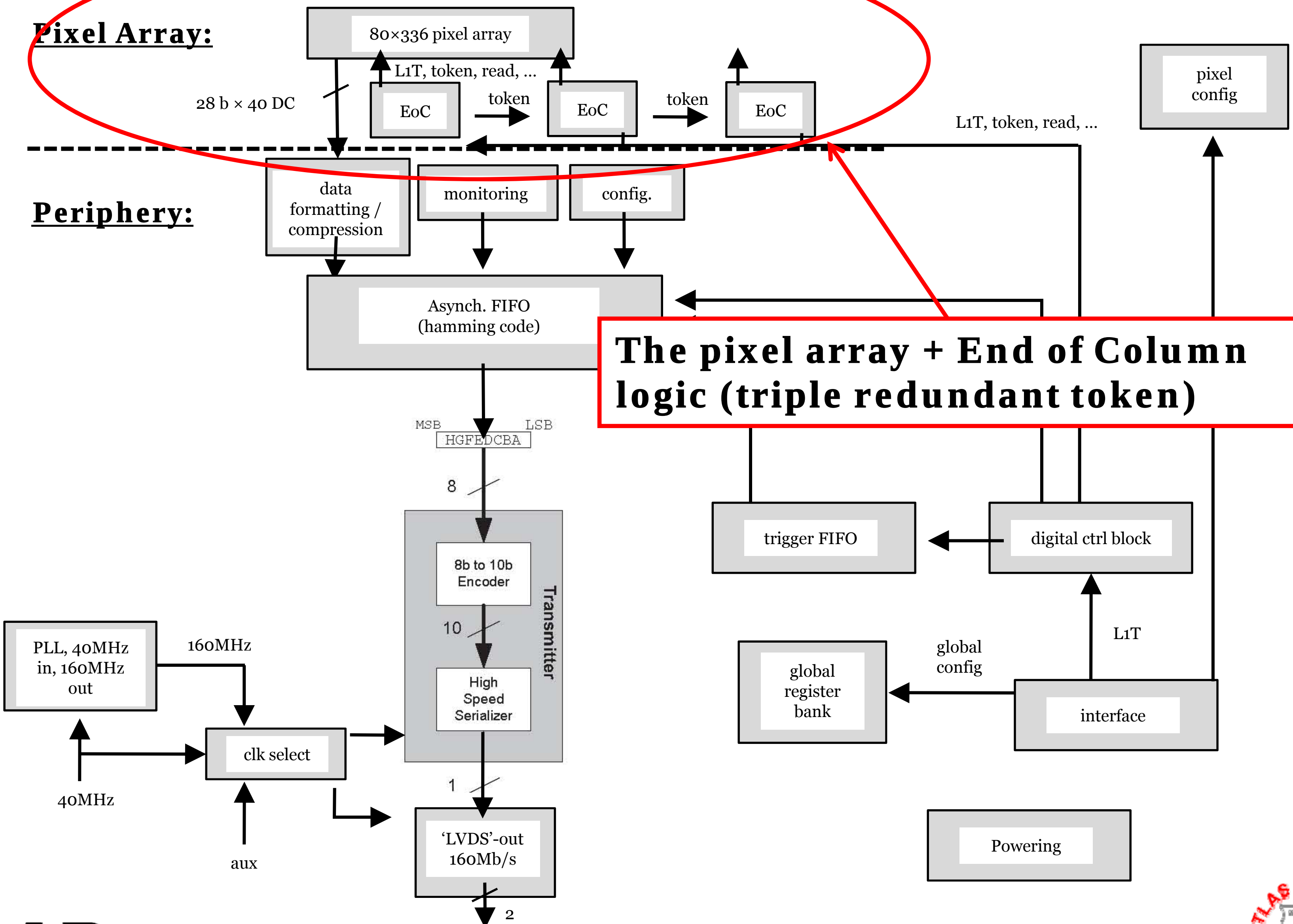




Power distribution and shield on top metals. Only vertical - no analog/digital crossing

Note: Digital ground tied to substrate, mixed signal environment BUT digital region placed in “T3” deep n-well.

FE-I4 Periphery



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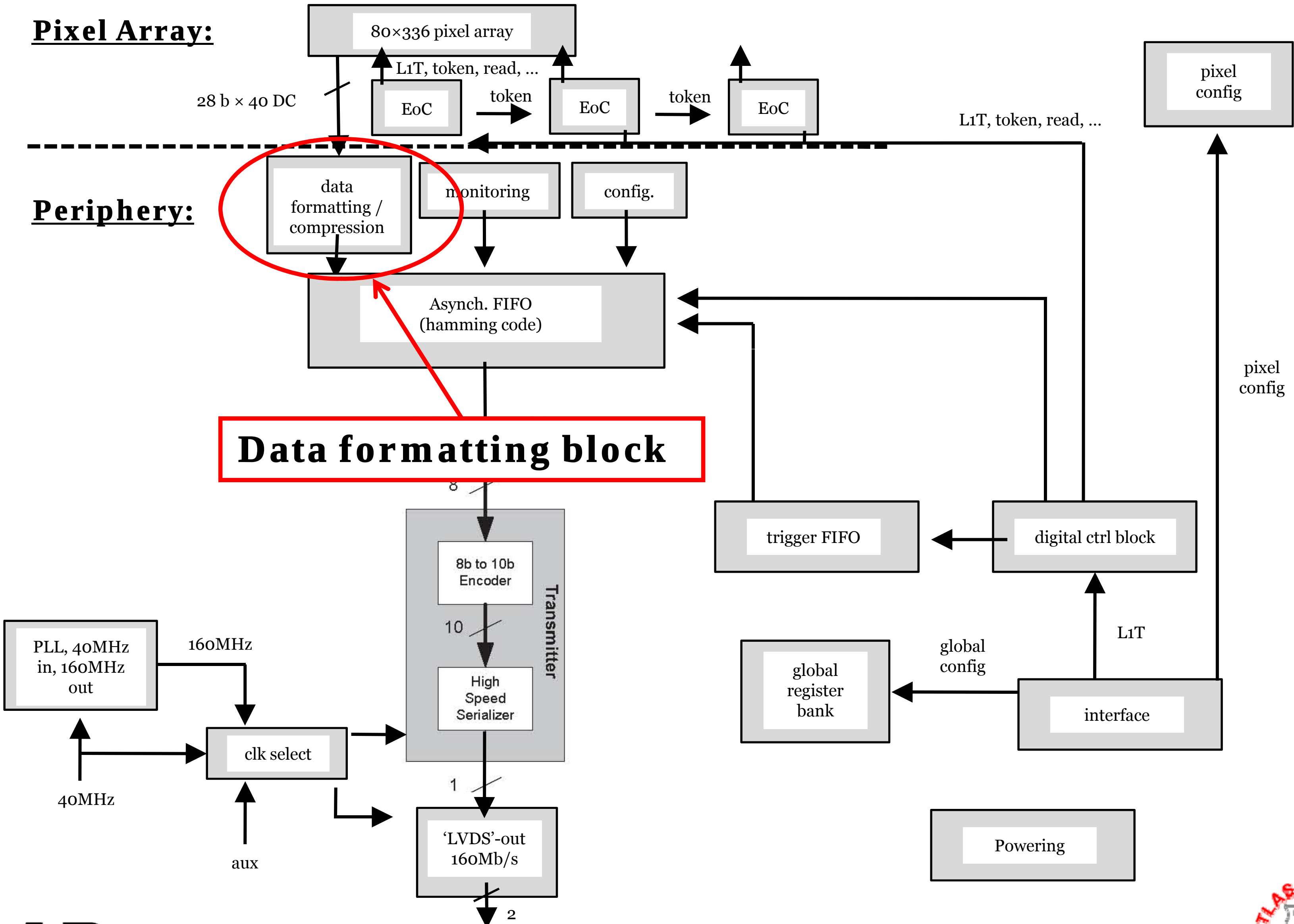

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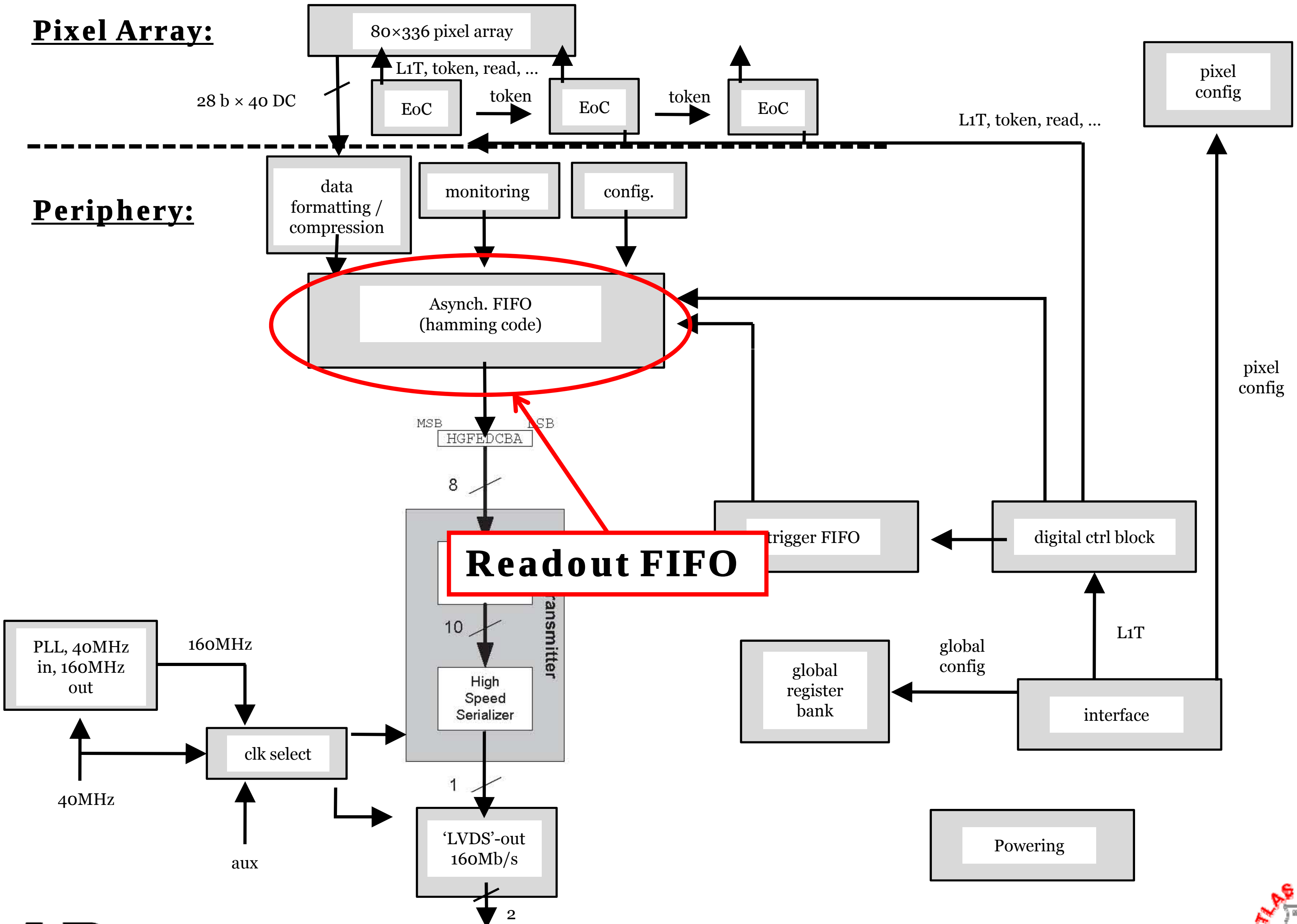

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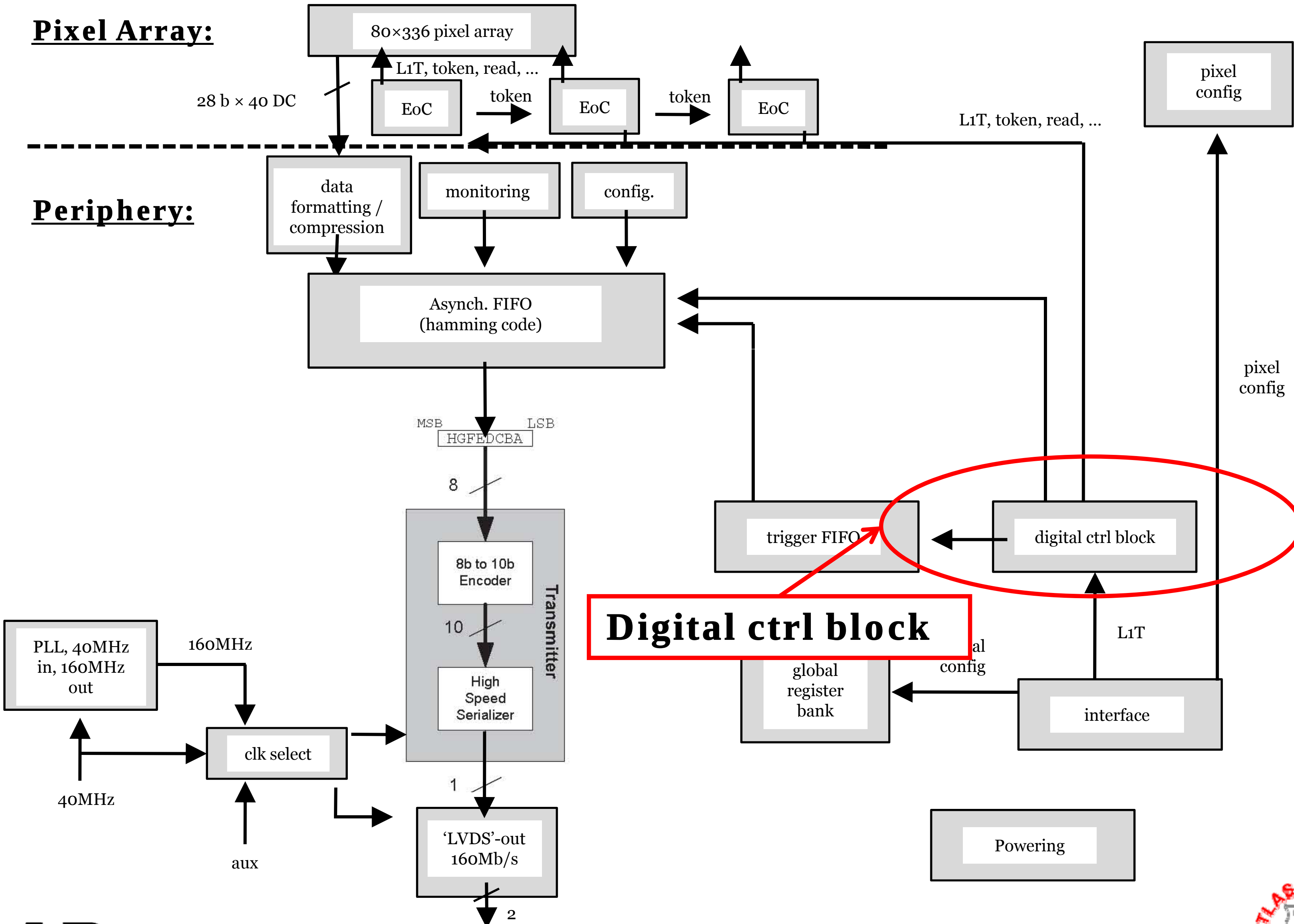

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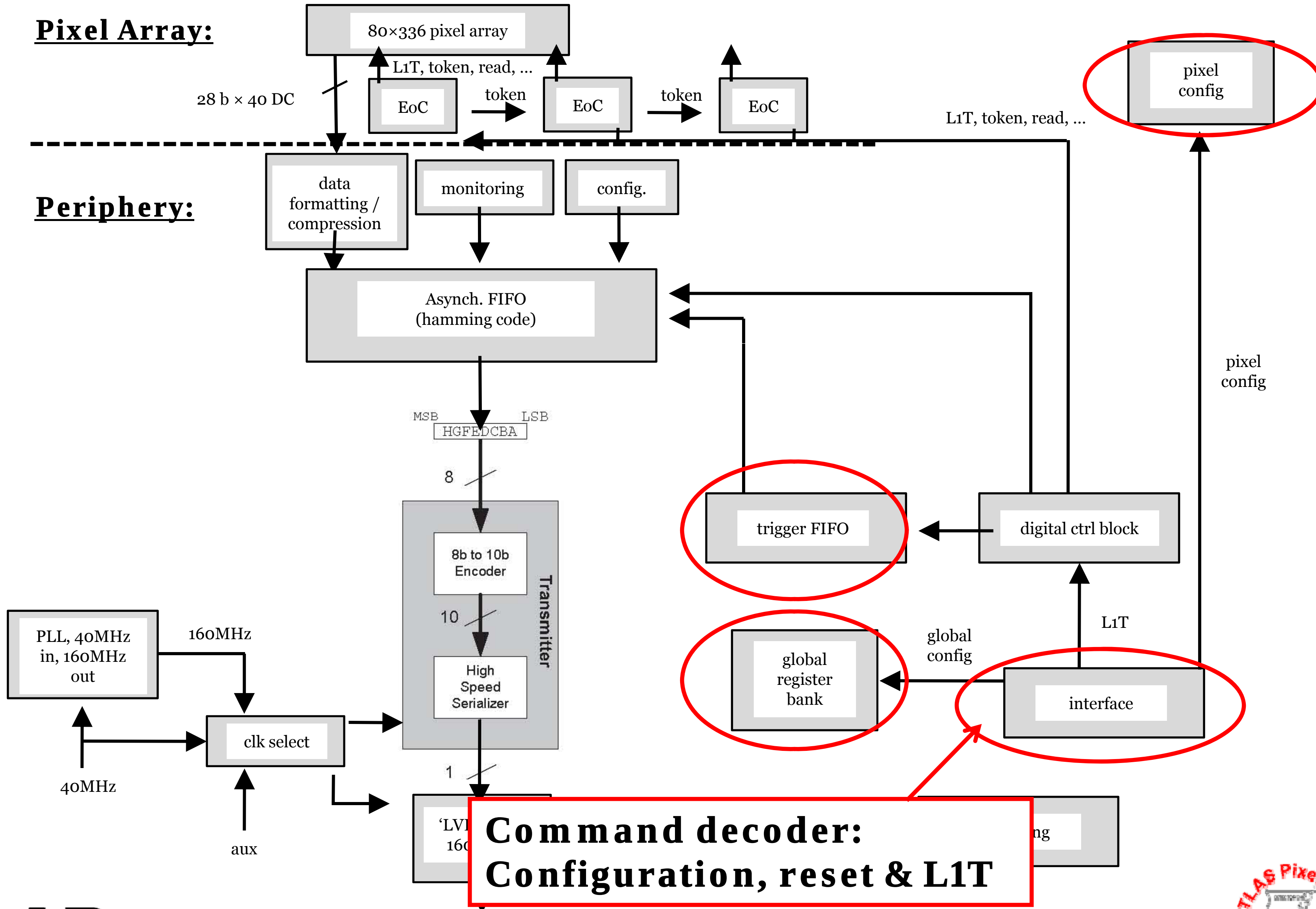

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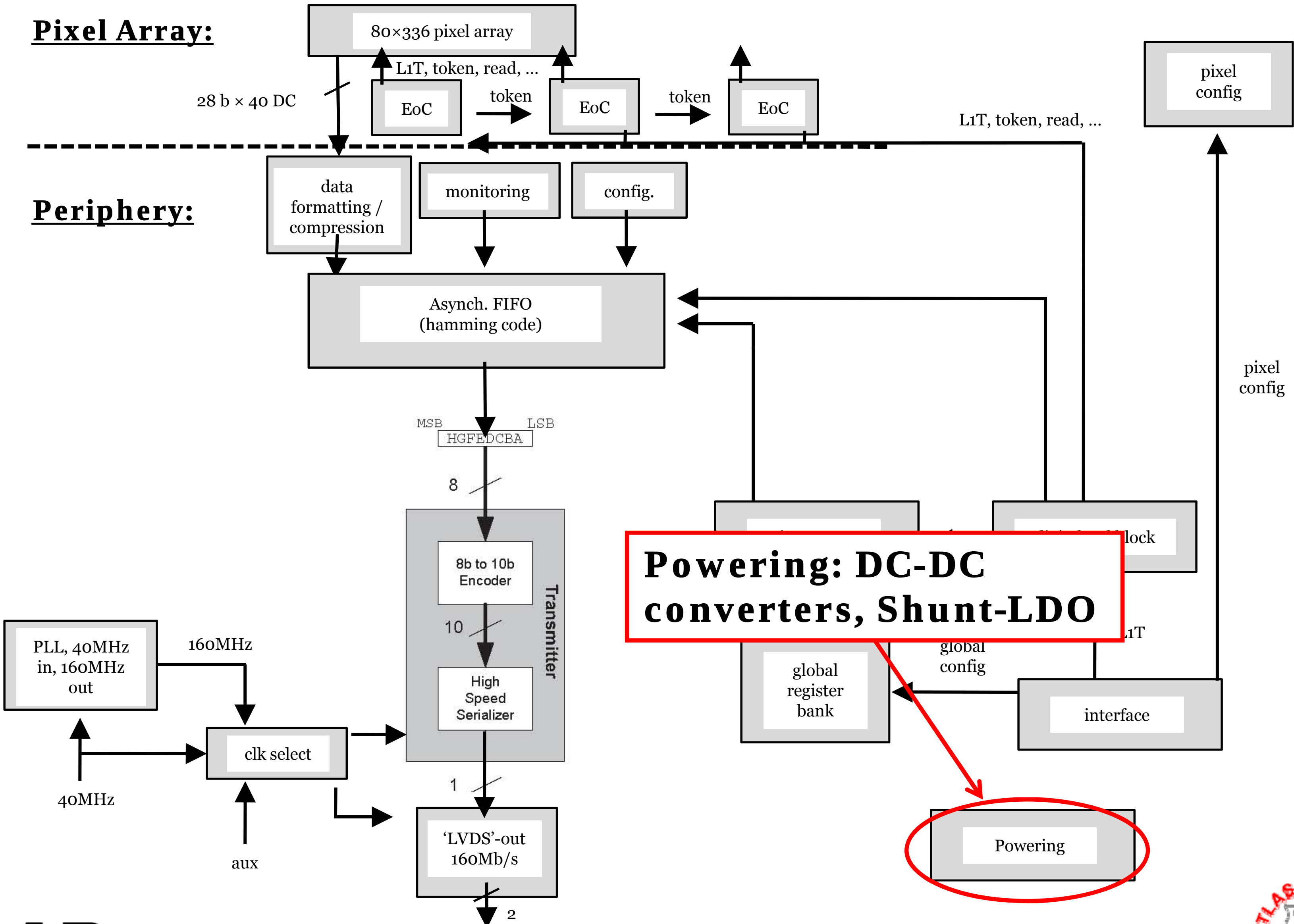

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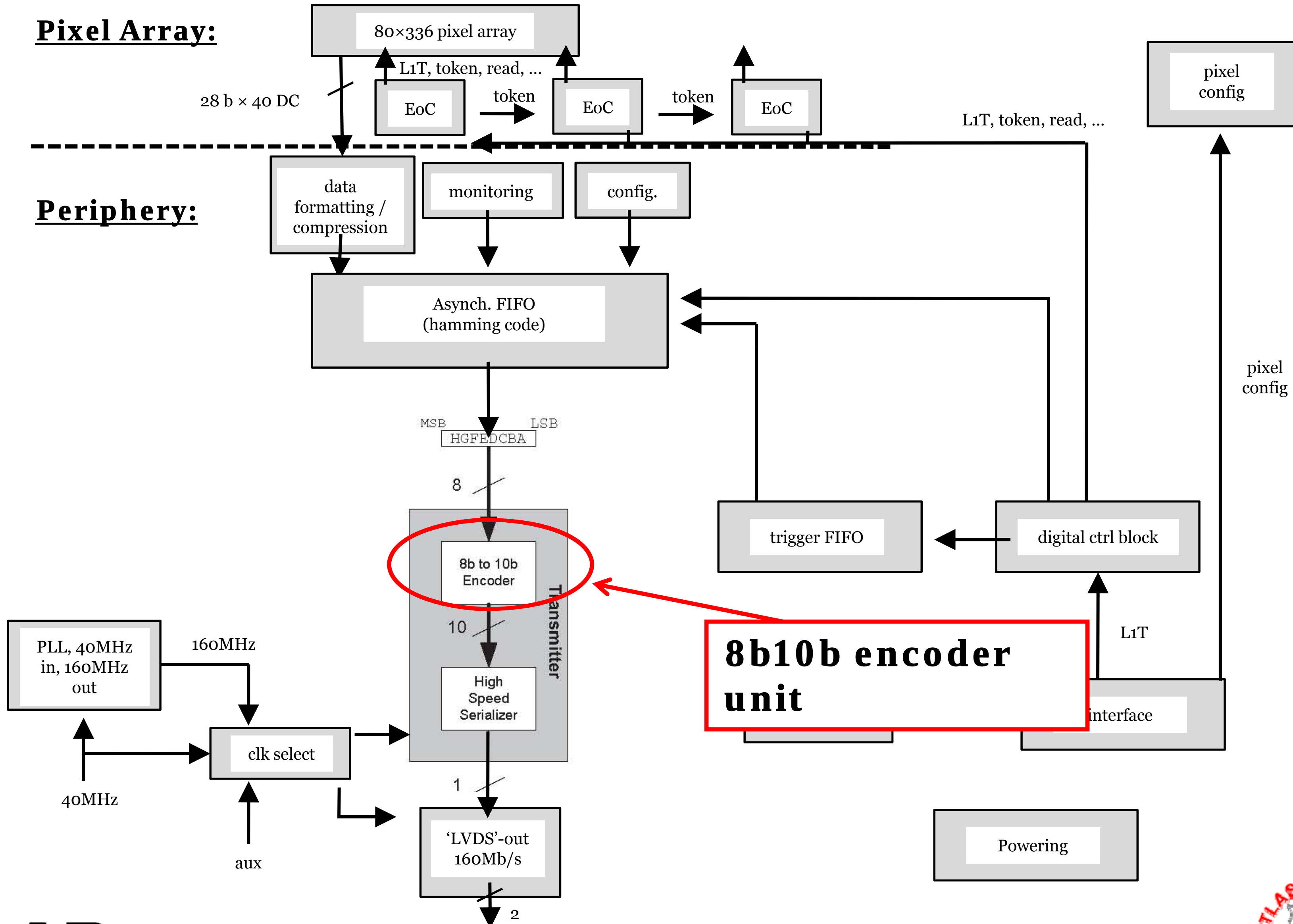

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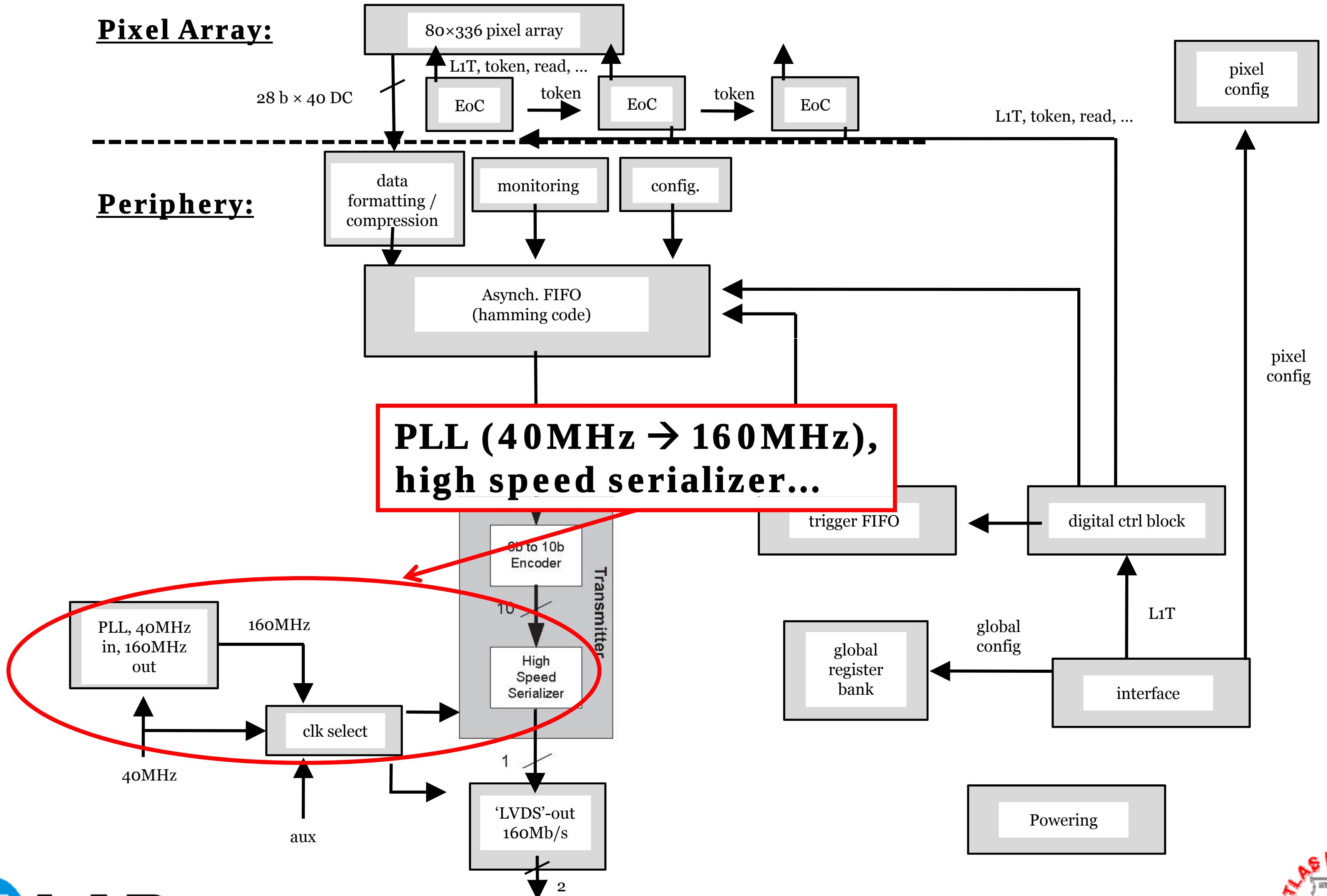

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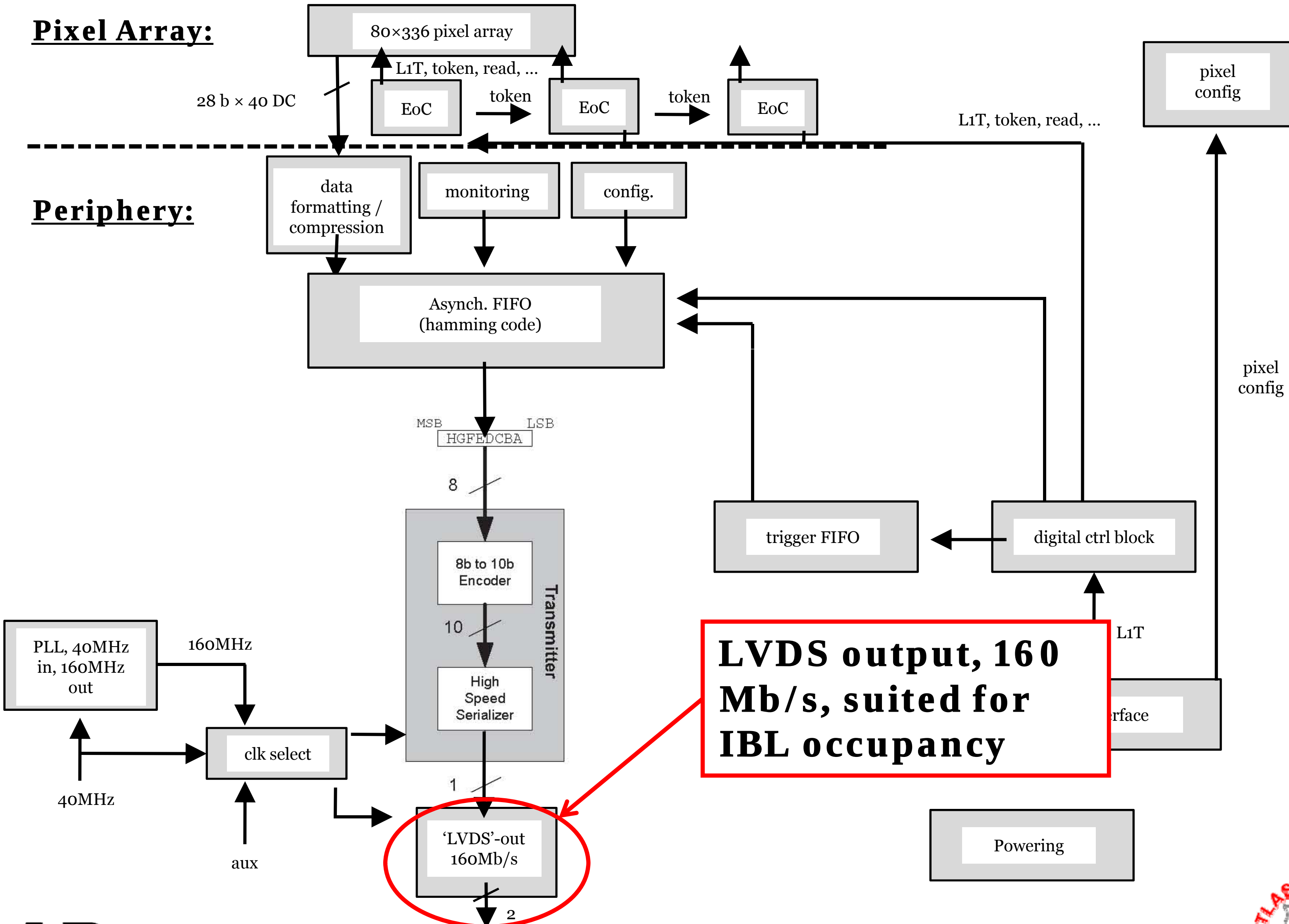


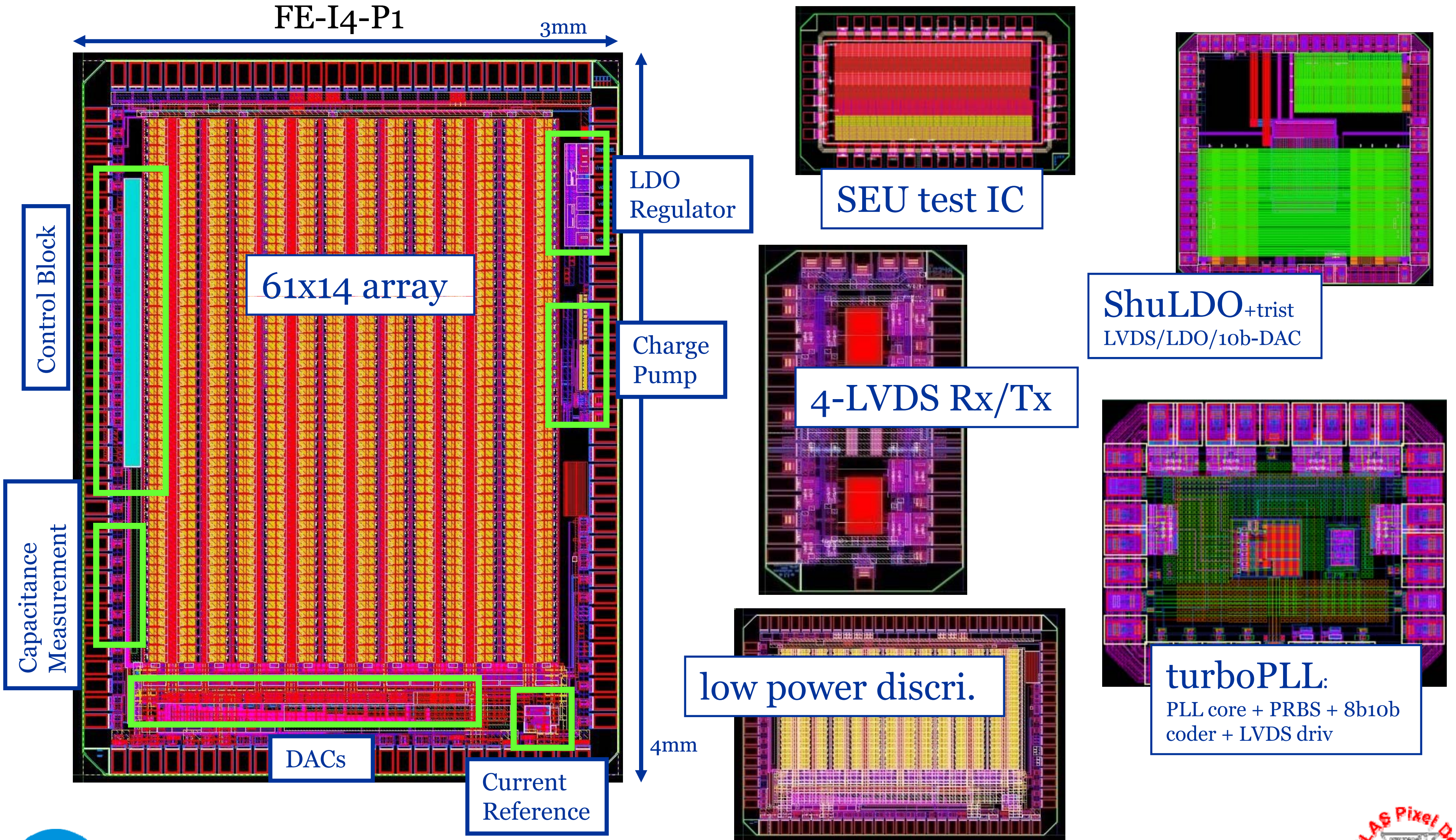
Yield

- Estimated from:
  - Small analog test chips.
  - 8 fully tested wafers of Medipix 3 ICs, assuming same defect density for synthesized logic.
- Expect of order ~39% digitally perfect chips.

- Yield enhancement:
  - Triple redundant read tokens.
  - Hamming coded pixel data and address (w. minimal # of gates).
  - Redundant configuration shift register.
- → Fully functional chips yield might be as high as 76%.

(with isolated dead pixels at level <0.1%).

Test Chip Submission



Schedule and more information

Schedule: Submission planned for End 2009
(submission readiness review 3-4 Nov. 2009)

- Few references:
  - "Development of the ATLAS FE-I4 pixel readout IC for b-layer Upgrade and Super-LHC", M. Karagounis *et al*, proceedings of TWEPP 2008.
  - "Design and Measurements of SEU tolerant latches", M. Menouni *et al*, proceedings of TWEPP 2008.
  - "New ATLAS Pixel Front-End IC for Upgraded LHC Luminosity", M. Barbero *et al*, submitted to Nucl. Instr. Meth. A, Sept. 2008.
  - "Digital Architecture and Interface of the New ATLAS Pixel Front-End IC for Upgraded LHC Luminosity", D. Arutinov *et al*, IEEE Trans. Nucl. Sci. 56, 388 (2009).
  - "An Integrated Shunt-LDO Regulator for Serial Powered Systems", M. Karagounis *et al*, Proceedings of the 35th European Solid-State Circuits Conference, 2009.
  - "Charge Pump Clock Generation PLL for the Data Output Block of the Upgraded ATLAS Pixel Front-End in 130 nm CMOS", A. Kruth *et al*, Proceedings TWEPP 2009.
  - "Low Power Discriminator for ATLAS Pixel Chip", M. Menouni *et al*, proceedings of TWEPP 2009.
- More information: Poster later this morning

"Digital Architecture of the new ATLAS Pixel Chip FE-I4" (Session N13, 'Posters I' Location: Grand Ballroom 4 / 5. Oct. 27, 10:30-12:00).

BACKUP SLIDES