

# Gigasensors for an Attoscope: Catching Quanta in CMOS

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## Silicon Takes the Stage in Particle Physics Experiments

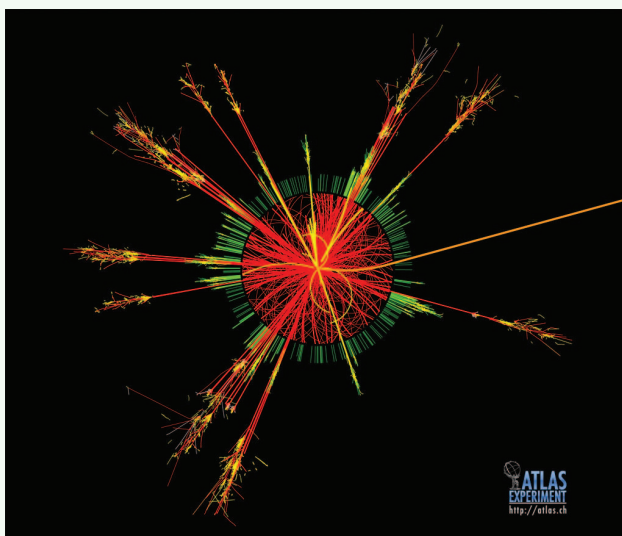
The gigantic experiments at CERN, the elementary particle accelerator laboratory in Geneva, Switzerland rely on custom-designed CMOS for much of their functioning. Close to a million CMOS chips, silicon-based sensors and other sensitive material, such as scintillating crystals or liquid argon, fill the space in and around a superconducting magnet, the size of a 6-stories building. The chips have to process small electrical signals, typically 10 to 20 thousand electrons, generated by the ionizing particles in the sensor elements. Silicon is sensitive to light, but very thick diode structures also deliver signals that are proportional to the energy loss of swift particles that pass through. The sensor cells have been connected in a fully parallel approach to their integrated read-out amplifiers and further signal processing, because the 'snapshots' of the successive interactions are uncorrelated, and take place every 25 ns: 40 million pictures per second. These massively parallel detector systems with close to  $10^9$  sensor cells have become possible only by exploiting the miniaturization of electronics.

The CERN experiments are situated deep underground along the 27 km circular accelerator called the 'Large Hadron Collider' LHC. Figure 1 gives an idea of such a collider detector, still under construction.



**Fig. 1** Part of the Atlas team assembled in between the end-caps, in the underground cave. Several thousand scientists and technicians have worked on the Atlas construction. The blue cylinder is a shielding block that surrounds the entry/exit of the not yet installed beam pipe. The magnet and the main barrel are to the left, invisible here. Photo CERN/Atlas.

The experiments study the fundamental physics processes between elementary particles at the highest momenta on earth. Particle beams circulating in opposite directions with thousands of bunches of protons are accelerated to 7 TeV, and then made to collide head-on in 4 crossing points. The experimental set-up around an interaction point consists of successive shells of different detectors in which one records all the effects in the miniature explosions that result when quarks inside these protons occasionally fuse together. Figure 2 illustrates the variety of reaction products in a rare, sought-after type of collision.



**Fig. 2** Simulated interaction in the Atlas detector with all outgoing reaction products traversing the successive shells of the detector. The central region where most particles are colored red, represents the inner tracker detectors. The surrounding heavy calorimeters provoke showering around the absorbed particles. The yellow track to the right is an escaping muon. The scale of the figure is ~10m across. Photo CERN/Atlas.

Only a tiny 'needle' fraction of the 'events' represent new physics phenomena, and these have to be filtered out from the majority 'haystack' of uninteresting data. A particle or quantum with 1 TeV energy has an equivalent wavelength of one attometer ( $10^{-18}$ m), compared to a micrometer for visible light, and so one can say that these experiments in the TeV energy range act as 'attoscopes' rather than microscopes, when they look at the properties of these energetic quanta on the atto-scale.

The introduction of silicon chips in particle physics experiments went by steps, and in this article I trace some of the history of silicon detectors and readout chips for tracking detectors. These form the inner shells of the equipment. As shown in Figure 2, they record the trajectories of the ionizing particles in a

somewhat similar way as cloud chambers, spark chambers or bubble chambers did in the earlier times. Although providing fewer measurement points along a track, the main advantage of the silicon tracker systems is the fully electronic operation and the ns collection time of the signals in the silicon layers. Already in 1976 at the EPFL, the Swiss Federal Technical University in Lausanne, during a workshop 'Limits on Miniaturization' my colleague Pierre Jarron and I became enthusiastic to apply developments in microelectronics for detection of particles. As shown in the next section, segmentation is the key to the silicon trackers, and in 1980 we introduced the silicon diode 'microstrip' detector with full parallel readout, following a visit at the nuclear physics institute IKO in Amsterdam. Then the design of custom chips for silicon detector readout was started at SLAC in 1981 and at CERN in 1986. Now, 25 years later a community of designers and users supply the various integrated circuits for detection and signal processing in the experiments at CERN, at Fermilab near Chicago, at the Stanford linear accelerator SLAC, and other facilities worldwide. The most recent development with 'ultimate' segmentation for particle tracking, ~ 1995, was the true 2D silicon pixel detector, for which Eric Vittoz and his coworkers in CSEM and at the EPFL contributed significantly, with advice, designs and training.

**Segmentation of Sensors, Serial or Parallel Readout**

The use of a contiguous array of segmented diodes on monolithic silicon for nuclear particle detection, as far as I know, was first proposed ~1961 by Leo Koerts from Philips/IKO in Amsterdam. Their 'checker board' detector with Schottky barrier strips on the front and orthogonal ohmic strips on the rear, both with 1.2 mm pitch, was described by Hofker in 1966 [1]. This was the device that Jarron and I took as the example for our silicon diode 'microstrip' detectors, with much smaller segmentation at 200 μm [2] and later at 50 μm pitch. The readout of the checker board was not yet fully parallel, but it had single analog amplifier channels, for front and rear of the sensor, together with a series of pick-up transformers for position determination along the diode array. The full system 'BOL' with 8000 'pixels' [3], operational 1968-1974, needed several cubic meters of electronics for this readout. It is interesting to remember that around this time monolithic 2D matrix approaches for imaging of visible light also were studied at Philips and at Bell Labs. Within a few years these proposed respectively BBD [4] and CCD [5] for imaging, and both approaches used serial signal readout.

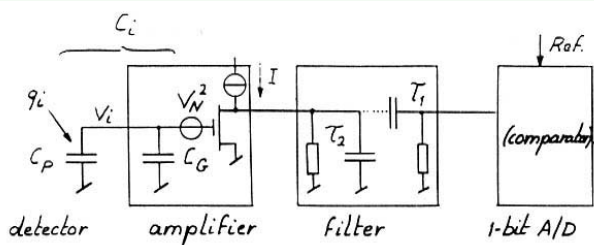
The earliest system with fully parallel readout for a sizeable array of sensing elements was the Multi-Wire Proportional Chamber (MWPC) for particle position measurement in 1968 [6] which earned Georges Charpak a Nobel prize in 1992. A separate amplifier connects to each wire and with a typical distance between wires of ~5mm, this electronics could be fabricated with the discrete components of the time. For the 'microstrip' detectors, made on kΩcm Si wafers by Schottky barriers and later by ion-implantation [7] at

first also discrete components were used for readout, but the need for integrated circuits now was obvious. Several teams initiated analog design work: Hyams, Parker and Walker started at Stanford with an NMOS chip, called Microplex [8]. Their design used a switched capacitor feedback amplifier and evolved later, thanks to Kleinfelder [9], Spieler [10] and coworkers at Lawrence Berkeley Lab into a family of CMOS chips, used still now at Fermilab in the CDF and D0 Tevatron collider experiments. In Germany, a team of the Munich Heisenberg Laboratory and the Duisburg Microelectronics Institute, with Lutz and Buttler, together with Manfredi et al. at the University of Pavia, developed a 128 channel CMOS circuit with JFET frontend transistors [11]. Later this chip was called CAMEX and was used in the electron collider experiment Aleph at CERN, from 1989 to 2001. All these circuits used a front-end amplifier with switching feedback and double correlated sampling, contrary to the continuous feedback in 'Amplex' that I will discuss in the next section.

But first more on the 'ultimate' segmentation: for the planned proton collider experiments in the USA and Europe, with their large number of simultaneous particles, from the early 1980's we at CERN wanted to push towards parallel sensor cells of micrometer dimensions in a true 2D matrix, using photolithography [12]. Damerell had shown the power of 2D measurements by using CCD [13] but the serial readout restricts this method to particular situations of low repetition rate or experiments where the beam can be stopped after an interesting interaction, such as in a linear accelerator. The question was, if we could implement conventional, ns signal processing and full parallel readout on a microscopic area with reasonable power dissipation. We approached Eric Vittoz with this question in 1986. For the first Workshop on Pixel Detectors in Leuven [14] Vittoz analyzed this problem, and he summarized some parameters in Table 1. Also he sketched the signal processing chain in Figure 3, and came with positive conclusions on

**Table 1**  
State of the problem

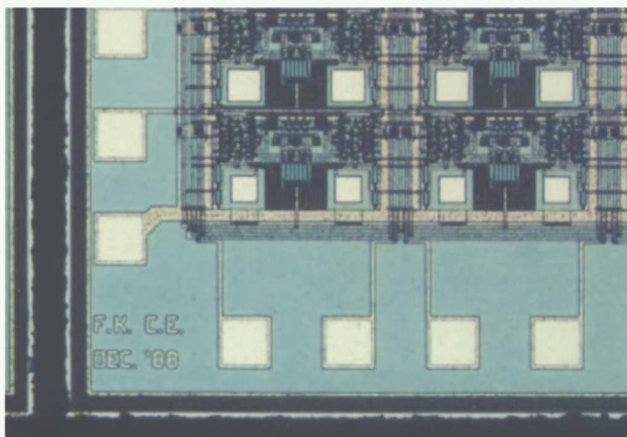
Total number of pixels	10 <sup>8</sup>
Pixel size	0.1 × 0.1 mm <sup>2</sup>
Chip size	50 mm <sup>2</sup>
Number of pixels per chip	5000
Number of chips in system	20000
Total system area	1 m <sup>2</sup>
Power per chip	10–100 mW
Total power	0.2–2 kW
Power per pixel	2–20 μW
Supply voltage	3 V
Current per pixel	0.7–7 μA
used for: amplifier; 1 bit A/D converter (comparator); multiplexer	
Cycle time (periodicity of events)	100 ns (10 MHz)
Nominal signal charge	10000 electrons
Intrinsic detector capacitance	4 fF per pixel
Total detector capacitance	
minimum: multilayer by SOI	10 fF per pixel
maximum: hybrid mount (flip-chip)	1 pF per pixel



**Fig. 3 Schematic by Eric Vittoz for the analog front end for an integrated pixel detector[14].**

power and noise. Such small pixels pinpoint positions of the particles in space with much better precision, but also have the pleasant characteristics of low capacitance and reduced dark current.

This allows low electronic noise, and recent matrices achieve  $\sim 100$  e- r.m.s.equivalent, at the input of the signal processing circuit, even with  $\sim 100$ ns signal shaping. The signal generated in the Si sensor by ionizing quanta is typically between 2000 and 20000 electron-hole pairs, so that one has a comfortable signal/noise ratio. In 1987 I dubbed these devices 'micropattern' detectors, because I imagined that eventually they would be able to recognize useful interactions from pre-defined patterns in the image. In practice the name 'pixel' detectors has now become the standard. In the English language, contrary to the French, there is an ambiguity between 'detector of patterns' and 'detector with patterns,' and the latter meaning has more recently been adopted in the field of gaseous devices.



**Fig. 4 Corner of the first pixel readout chip, showing 8 pixels with input contacts for bump bonding and some output pads for wirebonds. Design and layout by François Krummenacher and Christian Enz, Dec 1988. Made in SACMOS3 technology. Photo CERN.**

### The Earliest 'Micropattern' Pixel Detectors

In 1988, after the Workshop in Leuven, the design work started on a first prototype of a  $9 \times 12$  pixel detector matrix, by Smart Silicon Systems, a startup from the EPFL, with Christian Enz and François Krummenacher as designers, Eric Vittoz as adviser and the CERN team as the critical customers and users. With a future particle collider in mind some design choices

were made, such as a latched input circuit, in order to obtain low power dissipation. By Christmas the layout was ready, the chip was processed in the  $3 \mu\text{m}$  SACMOS technology at Faselec AG in Zurich. With self-aligned contacts (SAC) this technology offered increased density, allowing a small pixel area of  $200 \mu\text{m} \times 200 \mu\text{m}$ . In June 1989, after dicing at CSEM we made the microphoto of Figure 4, which shows one corner of the matrix with 8 input contacts and readout cells.

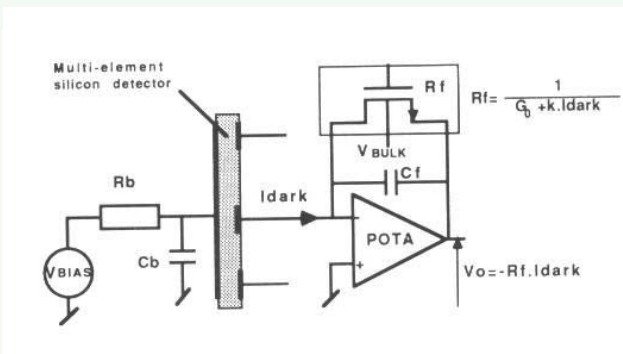
Michael Campbell and I made the first measurements over the summer, and our late paper was accepted for presentation at the 1989 Nuclear Science Symposium near San Francisco. The chip worked well, with noise below 500 e- rms, detection threshold  $\sim 3000$  e- and power of  $30 \mu\text{W}/\text{pixel}$ , all well below the design goals. But then some strange problems beset the first publication. The Symposium was cancelled because of the 17 October San Francisco earthquake. Despairing, we submitted the paper to Nuclear Instruments and Methods [15]. The Conference eventually was rescheduled in a different, undamaged hotel where Michael Campbell presented the paper only in January 1990 for a small audience. We also found that the planned bump-bonding could not be made because of a mm wide guard ring that is needed around the active sensor area, and this would obscure the wirebond pads on the electronics readout chip.

We initiated the design for a next chip, now aiming at an asynchronous input amplifier and a large, more practical matrix of 16 columns and 63 rows. The 64th row was dedicated to a provision for dark current compensation. Each pixel of  $75 \mu\text{m} \times 500 \mu\text{m}$  contained  $\sim 80$  transistors. The chip was again manufactured in the SACMOS3 technology, and after bump-bond assembly at GEC-Marconi in Caswell, the first particle tracks were measured at CERN on 20 October 1991. These measurements were presented at the 1991 Nuclear Science Symposium in Santa Fe [16], two years after those of the first chip. In the scientific community, with relatively modest resources long iteration times are typical, also because the design teams are involved in the development and testing of the full application system. Indeed, the following, third chip in this series was the LHC1/Omega3 [17], which became available early in 1995, nearly four years later. This chip with a  $16 \times 128$  matrix of cells used the SACMOS  $1 \mu\text{m}$  technology, which represented at the time a submicron component density in comparison with normal CMOS. The smaller pixel area of  $50 \mu\text{m} \times 500 \mu\text{m}$  could now contain as many as 400 transistors. I wonder if we can call this a 'hyper-active' pixel, after Eric Fossum just before [18] had claimed the term 'active pixel sensor' if each pixel contains at least one transistor. It may also be worth mentioning that the Faselec/Philips SAC1 process, although developed in Zurich, in 1994 just was transferred to the Taiwan Semiconductor Manufacturing Company TSMC, with the Swiss technology specialist J. Solo making many trips between Zurich and Taipei. That technology was never actually implemented anywhere at the Zurich foundry of Faselec, illustrating the

swift worldwide concentrations in microelectronics manufacturing. Only 10 years earlier, there still were several MOS factories in Switzerland, serving the local high-tech industries, described in the Summer Newsletter dedicated to Eric Vittoz.

### Active Feedback Compensates Dark Current

In semiconductor diode detectors, systematically one has to cope with the dark leakage current at reverse bias and often the input is AC coupled, in order to

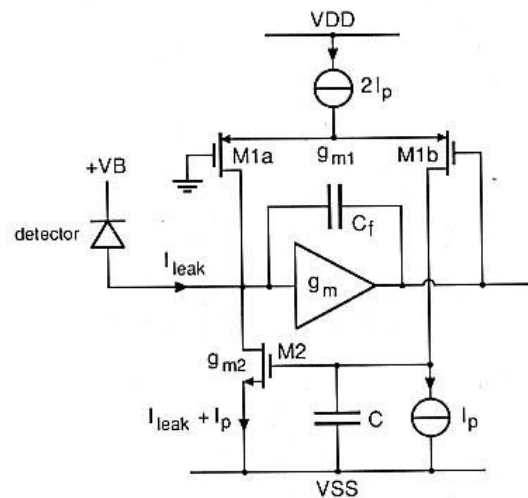


**Fig. 5 Schematic diagram of the connection of segmented diode elements to an Operational Transconductance Amplifier (OTA) with a feedback that restores the operating point if there is a large current  $I_{dark}$  at the input [19].**

avoid baseline shift and amplifier saturation. For highly segmented devices, external filtering networks become impractical and these have to be implemented on the silicon sensor itself. DC interconnections would be preferable, but then a scheme is needed to accommodate varying and sometimes large currents at the inputs of the front-end amplifiers. Sometimes hundreds of nA have to be compensated, even more after extended irradiation, although the current is strongly reduced by the sensor segmentation. For the gaseous detectors this is not an issue, because the gas remains a perfect isolator, even at kV bias.

At CERN, Pierre Jarron and I started in 1986 work on CMOS chip design for the segmented Si detectors with a training course in the INVOMECE division at the just founded IMEC centre in Leuven, Belgium. Jarron followed the nuclear electronics tradition, and implemented a continuous feedback scheme using a long transistor, as shown in Figure 5 [19].

With direct connection, the sensor dark current at the input modulates the effective resistance of the feedback, so that the operational level at the output can be maintained, at the cost of a slight reduction of amplification. A current up to 450 nA per segment can be compensated. The 16-channel AMPLEX chip [20] was produced in 1987 in the 3 $\mu$ m CMOS technology of MIETEC in Belgium. By chance this AMPLEX chip happened in 1989 to become the first integrated circuit to be actually operational in a beam collider experiment: the inner silicon array in the UA2 proton-antiproton experiment at CERN [21] was used a year before the vertex detector at the MARKII in SLAC was taking data in July 1990 [22] although the Microplex



**Fig. 6 Schematic diagram of the front end by Krummenacher with sinking of dark current via M2. This scheme can be implemented in each pixel [23].**

chip for SLAC had been designed some years earlier. The UA2 silicon detectors had a surface area of more than 1 m<sup>2</sup>, and this was at the time the largest silicon detector ever.

For the silicon pixel detector with their thousands of sensor cells and amplifiers, the DC coupling is the only practical possibility and a current compensation has to be implemented, on the small area available. In the Omega2 matrix Michael Campbell replicated the currents from a row of reference pixels. François Krummenacher proposed in 1990 a damped feedback illustrated in Figure 6 [23].

This can be implemented in each pixel, without the need for reference cells. The transistor M2 can sink the leakage current  $I_{leak}$ , and with proper choice of  $C$  and  $g_{m2}$  the tolerated  $I_{leak}$  can be much larger than the biasing current  $I_p$ . With thousands of pixels, in practical implementations a dark current as high as 1mA per cm<sup>2</sup> can be handled with this approach, and current fluctuations are slowly but automatically followed pixel by pixel.

### Massively Parallel 2D Gigasensor Array

The heart of three of the CERN LHC experiments is formed by several layers of true 2D pixel matrix detectors, which record at 40 MHz the positions and timing of all particles that pass through. Every single particle, representing a quantum of energy above the detection threshold of  $\sim 5$  keV is registered by these devices. The CMOS chips that are attached to the sensor matrix not only record the signals, but store these in local memory for up to  $\sim 4$   $\mu$ s, until a request for readout is received. Optical links could transmit a large fraction of the data but the off-detector data processing is designed for analysis of  $\sim$ kHz event rates, corresponding to expected numbers of interesting interactions. The actual sensitive area of the inner silicon pixel arrays ranges from 0.22 m<sup>2</sup> and 1200 chips in ALICE, to 1 m<sup>2</sup> with 16000 chips in CMS and 1.8 m<sup>2</sup> with 28000 chips in ATLAS. A much larger



**Fig. 7** Final assembly work on the Atlas pixel barrel (half). One can see the modules along the ladders. The white stubs are connecting tubes for the cooling channels, one for each ladder. Photo CERN/Atlas.

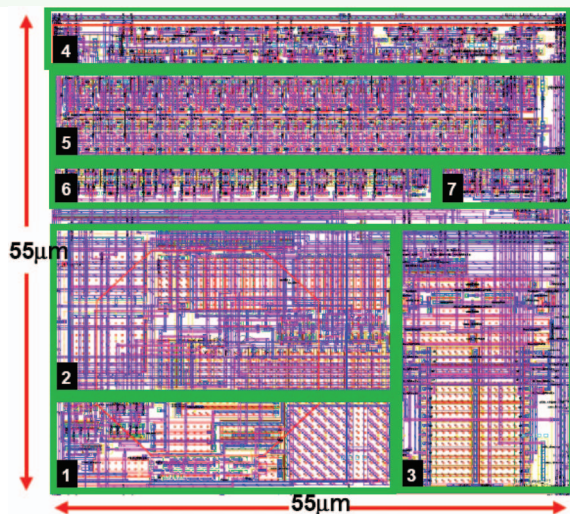
area, up to 400 m<sup>2</sup>, is covered in the next shells with 1D silicon microstrip detectors. Also these detectors employ tens of thousands of CMOS chips for the signal readout and data processing. At the start of the LHC the overall number of pixels per experiment is not quite 10<sup>9</sup> yet. It is expected that a higher beam intensity in a couple of years will bring a need for upgrades with more pixel layers, to replace the currently installed layers of 1D silicon microstrip detectors. If the particle density in each beam crossing is increased, the projective 1D detectors can not cope with the ambiguities between several coincident particles anymore, and true 2D detectors are necessary.

It is not possible here to describe in detail all aspects of these complex systems, such as the data readout systems, the power distribution (~ 50 kW for the inner silicon detectors) and the cooling. Figure 7 gives an impression of the pixel detector for ATLAS, showing half of the barrel under final construction.

This device will sit tightly around the beam pipe, detect millions of particles per second and undergo a large amount of radiation over the planned lifetime of ~10 years. The survival of the CMOS as well as the silicon sensors has been studied and the use of standard technologies has been found acceptable. The unavoidable increase of sensor dark current and the changes of material properties can be mitigated by operating the detector well below 0 degree C. With the installation completed, the number of dead sensor elements is still below 1%, and the 'giga' detectors are practically ready to take beam.

### Some Future Developments

The increased density in CMOS allows to integrate ever more functionality in each pixel while keeping dimensions of some tens of μm. This can improve precision in space and time for particle experiments. Eventually, trigger selectivity may profit if signatures for useful interactions could be determined. In other fields of science various new applications of particle detectors begin to appear. For example, pixel arrays are now used for X-ray imaging with individual processing of each incoming photonic quantum. This



**Fig. 8** Layout for the Medipix3 chip of a 55μm pixel cell in a 130 nm CMOS technology. Pre-amplifier, shaper and comparators, resp. 1, 2 and 3 form the analog part, while 3-7 are the control logic, counters, configuration and arbitration circuits. This pixel has more than 1080 transistors [25].

allows selection of energy bands and representation of the image in different "colours." Thresholding eliminates various types of background and long exposures can be made, such as needed with low intensity, nanofocus X-ray sources. Our group at CERN, with Michael Campbell as team leader, has designed the family of 'Medipix' imagers [24], building on the expertise in ionizing particle detectors. Figure 8 shows the layout of a pixel in the Medipix3 readout chip [25], the first particle detector where each pixel communicates in real time with all of its neighbours, to compare and add up coincident signals that belong to the same incident radiation quantum.

The Medipix chips are 3-side buttable, and the construction of a large area array will be needed to allow for use in medical applications. For a CT scanner a detector array of ~m<sup>2</sup> may be required. With ~ 50 000 pixels per cm<sup>2</sup> then such a device also will present close to 10<sup>9</sup> sensor cells, another gigasensor.

In conclusion, CMOS chips in conjunction with silicon diode matrices are now used on a large scale for ionizing particle imaging. They are catching quanta in physics experiments as well as in X-ray imaging. Eric Vittoz has been instrumental in guiding the early developments leading to these gigasensors. Not only computing and consumer electronics but also various branches of science can profit from the progress in microelectronics.

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## About the author



**Erik Heijne** (F '77) studied physics at the University of Amsterdam, where he assisted in projects on hydrogen/deuterium in palladium (1969) and on quantum effects in thin silicon films (1970). He came to CERN in Geneva in 1973, to work on silicon detectors for the monitoring of the neutrino beams. In 1980 the introduction of the silicon microstrip detector opened new ways for charm and beauty physics. A stay in Leuven (B) in 1984 led to the start of a microelectronics design group at CERN. Learning through different contacts in the IEEE, around 1995 he introduced at CERN the ideas for radiation hardness by design, which eventually became the basis for widespread use of CMOS in collider experiments. He is a Fellow of the IEEE and in 1999 received the Merit Award of the IEEE Nuclear and Plasma Sciences Society.