

Design Considerations for High Step-Down ratio Buck Regulators

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Abstract

The buck or step-down DC-DC converter is the workhorse switching power supply topology. It utilizes two switches (two FETS or one FET and one diode) along with an output inductor and output capacitor.

Whether you look at a large computer server, a personal desktop or a laptop computer, a cell phone or a GPS unit all will contain a buck converter in one form or another. This paper will discuss the synchronous buck topology, design considerations, component selection followed by a small signal model of buck converter. Issues that are important in optimizing the efficiency of the design for example MOSFET selection, the impact that the MOSFET driver plays in improving the efficiency will be examined. The paper will finish by contrasting various control architectures.

I. INTRODUCTION

As already mentioned, the buck converter steps down the input voltage from a high voltage to a low voltage. The simplest way to reduce the input voltage is to use a voltage divider circuit, but this is very inefficient and the excess voltage is wasted as heat. The buck converter provides an alternate voltage reducing method that minimizes the energy wasted and is highly efficient

Referring to Fig 1, the buck converter does this by alternately turning on and off the two MOSFETs Q1 and Q2 at a specific frequency resulting in chopped version of the input voltage appearing at the common connection point (referred to as Switch node) of the MOSFETs. The chopped voltage is followed by a low pass filter consisting of an inductor L1 and a capacitor Co. A dc voltage equal to the average value of the chopped voltage appears across the capacitor, while the ac voltage appears across the inductor. By balancing the volt-second across the inductor, the input-output conversion ratio of the buck converter is found to be “D” which is equal to V_{out}/V_{in} . This is referred to as dc gain of the converter.

Buck converter is the basic building block that drives the power electronics. Various forms of step-down converters exist, in both non-isolated and isolated forms. Isolated versions of the buck converter include push-pull bridge and forward topologies.

Prior to selecting the design approach, it is critical to understand the system needs/specs and design limitations

Considering the switching behaviour of MOSFET is critical in order to evaluate the conduction and especially the switching losses associated with the topology.

Output inductor is another very important part of the design selection, and compromises have to be made based upon loop performance, core and copper losses.

The paper will review the various controller architectures and summarize the pros and cons of each approach

II. SYNCHRONOUS VS NON-SYNCHRONOUS BUCK

Switching or Inductive buck converter as shown in fig. 1 provides higher efficiency. Q1 is referred to as control Fet and Q2 is referred to as synch Fet.

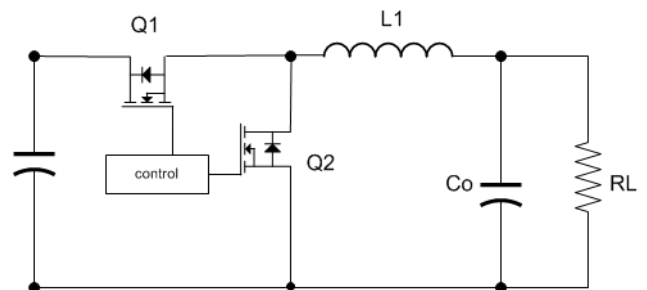


Fig 1 – synchronous buck converter

Note with 7% improvement in converter efficiency, Output power doubles for fixed power dissipation. From the system point of view it is critical to have a converter that has high efficiency, thus the overall system cost can be reduced as less efficient design will require extensive thermal management.

A non-Synchronous Buck converter (when Q2 is replaced with a diode D2) has two operating modes. At high load current it is in continuous conduction mode (CCM). As the load current decreases it goes into discontinuous conduction mode (DCM). During discontinuous mode (DCM) of operating catch diode (D2) blocks reverse current and voltage across the inductor is collapsed. During DCM there is an interval where no current is passed to the output inductor. Thus the average inductor current provided to the load requires a more detailed analysis. Whereas Synchronous buck converters will always operate in continuous conduction mode as the Sync Mosfet is turned on allowing reverse current to flow. Synchronous buck converter will tend to provide higher efficiency at high loads

because of sync MOSFET with low On-resistance will result in lower conduction losses than diodes. In order to improve efficiency at light load conditions the converter is allowed to operate in DCM. This is generally done by turning off the sync FET when negative inductor current is sensed. Circuit emulates diode behaviour under this condition.

III. SPECIFICATIONS/ DESIGN CONSIDERATIONS

Before designing any converter topology, it is important to determine the system specifications. The input voltage range, output voltage, load current, output ripple voltage and load transient requirements are typically specified by the customer. Other typical specifications relate to space and thermal constrains.

Space and thermal constrains typically determine the frequency one would design the converter to operate at. Operating at higher frequencies the size of output components ie. Inductor and capacitors will tend to get smaller, but on the other hand operating at high frequency will also tend to increase the switching losses in MOSFETs, Fet Driver circuitry etc. Thus a compromise is required that would tend to meet the size constrains as well as meet the thermal/ cost targets of the design. Buck topology is generally the most cost effective approach due to the low component count.

Table 1: Typical Specifications

	Min	Max	Tolerance	Req'd
Vin	3.3	15		
Vout	1.8		+/- 3%	
Iout	0A	10A		
Output Ripple		50mV		
Transient		100A/u-sec	+/- 100mV	
Size		H x L x W		
Efficiency	85%			
Ambient temperature		55C		
Enable				x
Tracking				x
OV protection				x
Current limit				x
Cost Target				

The input capacitor to the buck converter is selected based upon the input ripple current that the capacitor will see in the design, along with ensuring that it meets the voltage/ size requirements for the design. Rms value of input capacitor ripple current I_{cin_rms} can be estimated as indicated below.

$$I_{cin_rms} = I_o \sqrt{D(1-D)}$$

Where duty ratio D is defined as output to input ratio and referred to as "dc" gain of the converter.

$$D = V_o / V_{in}$$

For high duty ratio, i.e. for output voltages that are close to the input, for example Vout = 9V for Vin = 12V a PWM controller must be picked that is capable of operating at high duty cycle. This constrain is typically specified in the data

sheet as either the maximum duty cycle or the minimum off time of the top MOSFET.

For high step-down, where there is a wide separation between input and output voltage for example if Vout = 0.8V and Vin = 15V the PWM controller must be capable of operating at very low duty ratio i.e. min duty cycle. The datasheet of the controller will typically specify this as a minimum on-time for the top MOSFET. The minimum on-time specification will determine the maximum operating frequency of the converter for the specified input and output voltages while taking into consideration the efficiency of the design.

IV. MOSFET SELECTION

There are a number of factors that are critical to ensure high efficiency. Proper component selection i.e. MOSFET, Output inductor, Optimum drive voltage driving the MOSFET, reduced dead time and careful layout all play a major role in the final design to ensure high efficiency.

In order to ensure that the converter provides high efficiency, proper MOSFET selection is critical for the design. As MOSFETs are one of the major loss contributors of the design.

There are a number of MOSFET critical parameters besides Rds(on) and Qg that must be evaluated i.e. Cgd, Cgs and Cds, but these are not readily defined in the FET datasheet, but can be calculated as follows:

$$C_{GD} = C_{RSS}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS}$$

These parasitic capacitors of MOSFETS are related to the actual geometry of the device. Junction capacitors of semiconductor are non-linear and are inversely proportional to Voltage as indicated below. If we evaluate the charge in capacitor, one can see that the charge at some arbitrary voltage Vin will be twice as much as compared to the charge that a linear capacitor will have at voltage Vin.

$$C = f(V_c) = C_o \sqrt{\frac{V_{rest}}{V_c}}$$

$$C_{gd}(Vin) = 2C_{rss_spec} \sqrt{\frac{V_{ds_spec}}{V_{in}}}$$

Forward transconductance of the MOSFET is its small signal gain in the linear region of operation. The transconductance, gfs, is relationship between Drain current and gate-source voltage.

$$g_{fs} = \frac{dI_D}{dV_{GS}}$$

For high speed switching applications, MOSFET Gate resistance along with Gate driver resistance is extremely critical especially for high speed switching applications.

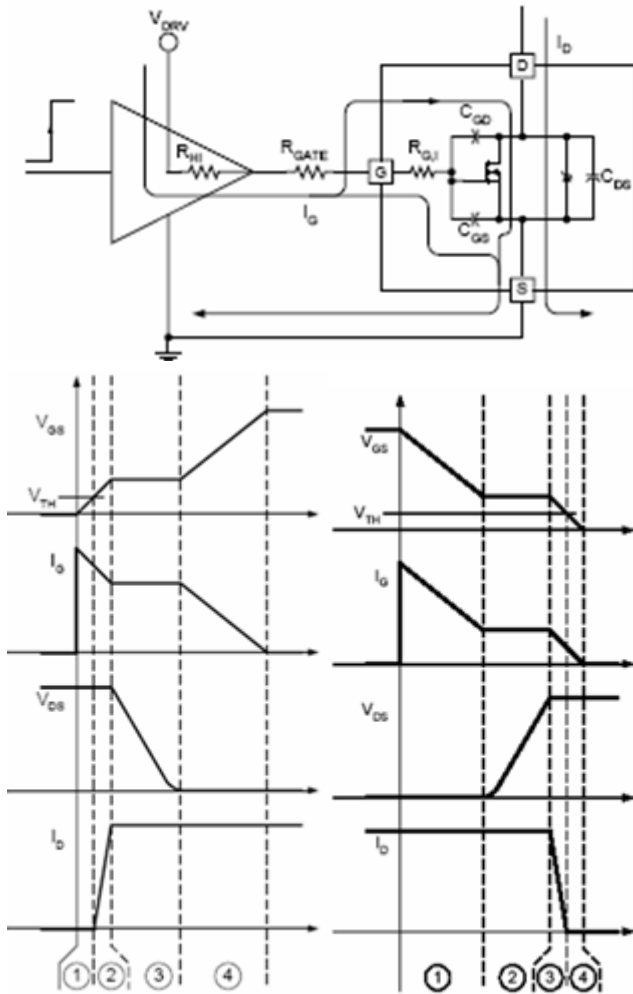


Fig 2 MOSFET turn-on / turn-off behaviour Ref [2]

Turn-on behaviour of buck converter, based upon conventional model can be broken down into four steps. In the first stage, the input capacitor of MOSFET is charged from 0V to V_{th} , during this phase gate current is charging the C_{gs} capacitor. This phase is referred to as turn-on delay as drain current and drain voltage remain unchanged.

In the 2nd stage gate is raised from V_{th} to Miller plateau. This is the linear operation of device, when the current is proportional to gate voltage. Gate current is flowing in C_{gs} and C_{gd} capacitors here the drain current is increasing and V_{ds} voltage does not change – in off state. This is the time it takes the MOSFET to carry the entire inductor current.

In the 3rd stage drain voltage is allowed to fall. While drain voltage falls, V_{gs} stays steady. All the gate current from driver is diverted to discharge the C_{gd} capacitor, in order to facilitate rapid voltage discharge from V_{ds} . Drain current in device stays constant, as it is limited by external circuitry.

In the 4th stage MOSFET channel is fully enhanced by applying higher gate drive voltage. During this phase gate voltage is increased from V_{gs_miller} to its final value. This determines the ultimate on resistance of the device. During this phase gate current is split and charges C_{gs} and C_{gd} . On resistance is reduced.

Turn-off behaviour is similar to turn-on behaviour and is subdivided in four stages.

In the first stage, turn-off delay, during this phase C_{iss} capacitor is discharged from its initial value to the Miller plateau level. Current is flowing thru C_{gs} and C_{gd} capacitors of Mosfet.

In the 2nd stage V_{ds} rises from $I_d \cdot R_{ds}$ on level to $V_{ds(off)}$. This period which corresponds to Miller plateau of the gate voltage. During this phase gate current is the charging current of C_{gd} capacitor and is subtracted from drain current.

In the 3rd stage gate voltage starts to fall from V_{gs_miller} to V_{th} . Majority of current is coming out of C_{gs} capacitor, as C_{gd} capacitor is virtually charged from previous stage. MOSFET is in linear mode declining gate-source voltage causes drain current to decay and reach zero by end of the interval.

In the 4th stage turn-off stage is to discharge the input capacitor of the device. V_{gs} is further decreased and most of the current is coming out of C_{gs} capacitor.

Profile of losses in both high side and low side Mosfets are quite different, especially for low output voltages where duty cycle is low. For low duty cycles low-side Mosfet are dominated by conduction losses.

$$P_{conduction_HS} = I_{q\ rms_HS}^2 R_{ds\ on} = I_o^2 R_{ds\ on} D$$

Power Losses in Synchronous buck regulator consists of conduction losses, switching losses, Gate losses, C_{oss} losses (Power loss to charge the MOSFET's output capacitor) this loss is dissipated in the R_{ds} of the MOSFET.

In order to minimize switching losses, turn-on and turn-off transitions as highlighted in stage 2 and stage 3 of waveforms must be minimized. These transition times are when the MOSFET is in its linear operation range, when the gate voltage is from V_{th} to V_{miller} . Gate driver's ability to source and sink current are critical in determine the switching times.

Source Gate current during turn-on transition t_2 can be approximated by I_{g_t2} and source gate current during (sink) turn-off transition t_3 can be approximated by I_{g_t3} . Switching times can be approximated by Q_{g_sw}/I_g . Switching losses

$$P_{sw} = (1/2)V_{in}f_{sw}\{[I_{q\ min}t_2] + [I_{q\ max}t_3]\}$$

$$I_{q\ min} = I_o - \Delta I_{L1}/2 \quad I_{q\ max} = I_o + \Delta I_{L1}/2$$

MOSFET driver losses can be approximated as $P_{sw_drv} = V_{drv}f_{sw}Q_g$ where Q_g is total gate charge.

Output capacitor losses; note C_{oss} is non-linear capacitor and voltage dependent. $P_{cos\ s} = 0.5C_{oss}f_{sw}V_{in}^2$ and diode reverse recovery losses $P_{Qrr} = Q_{rr}V_{in}f_{sw}$.

If external Schottky diode is used then during high side MOSFET turn-on, schottky's external capacitor needs to be charged. Schottky diode losses $P_{schottky}$ can be calculated as

$$P_{schottky} = C_{sch}V_{in}^2f_{sw}/2$$

V. MAGNETICS

MOSFET Gate current during turn-on transition t_2 can be approximated by eq (1), gate current during turn-off transition t_3 can be approximated by eq (2) and the switching times t_{sw} , t_2 , t_3 can be approximated by eq (3).

$$Q_{g_sw} = Q_{gd} + 0.5Q_{gs}$$

$$I_{g_t2} = \frac{V_{drv} - (V_{th} + (I_{qmin}(1/g_m)))}{R_g + R_{gext} + R_{drv}} \quad (1)$$

$$I_{g_t3} = \frac{V_{th} + I_{qpk}(1/g_m)}{R_{gfet} + R_{gext} + R_{drv}} \quad (2)$$

$$t_{sw} = Q_{gsw}/I_g \quad (3)$$

$$P_{conduction_LS} = I_{q_{rms_LS}}^2 R_{ds_{on}} = I_o^2 R_{ds_{on}}(1-D)$$

For the synchronizing fet (low side Mosfet) the major contributor is the conduction losses especially for low output voltages. As the MOSFET conducts current for the major part of duty cycle. Switching losses in the low side MOSFET are practically negligible, since Q2 switches on and off with a diode drop across it.

Conventional model which is commonly used in analyzing buck converters can give one simple and quick estimated losses. But for practical applications, efficiency measurements can provide better indications, when comparing one fet as compared to another. One of the main drawback of using conventional model is that it does not take into account the effect of source and drain inductances. These are package related parameters and play a significant role especially when operating at high frequencies. Reference [10] highlights the impact of source and drain inductance in the model. Model when taking leakage inductance into considerations shows that the turn-off losses are significantly greater than the turn-on losses, and measured and calculated error in switching losses is reduced.

High side MOSFET is selected to have low Q_g , whereas Low side (Sync) MOSFET is selected to have low $r_{ds\ on}$ since for low output voltages, sync fet conducts for higher duty cycle, thus conduction losses are the dominant factors.

MOSFET driver plays a significant role in determining the efficiency of the circuit. $R_{ds\ on}$ of MOSFET is inversely proportional to gate drive voltage V_{gs} . This can be observed in any MOSFET data sheet, thus higher drive voltage results in lower $R_{ds\ on}$. Typically drive voltage of approx 7V provides the optimum efficiency. This is the reason, one tends to see most design operating at drive voltage of approx. 7V, when input voltage is 12V. When the input voltage is reduced to 5V or below, the internal linear regulator which typically provides 7V drive voltage is bypassed and the drive voltage used to drive the MOSFETs is the input voltage. Thus ensuring higher efficiency. MOSFET must be driven from a low impedance source that is capable of sourcing and sinking adequate current to ensure fast switching. Current source and sink capabilities of MOSFET driver must be capable of sourcing and sinking adequate current to ensure fast switching transitions.

Output inductor is another critical component of the design. It is important that the inductor is designed to ensure that it does not saturate when under the operating or overload condition of the circuit.

Inductor must be designed to ensure that the losses are not exceeded that would result in saturating the inductor implying that the inductance is reduced in the circuit.

There are two classes of materials used in inductors – One is alloys of iron and contain some amount of other elements i.e. silicon (Si), nickel (Ni), chrome (Cr) and Cobol (Co).

Other type of material is ferrites. Ferrites are ceramic materials. Mixture of iron, manganese (Mn), zinc (Zn), nickel and cobolt. Ferrites have high resistively.

Iron powder is obtained from iron with low carbon content. Iron powder is resin bonded. Powdered iron cores consist of small iron particles electrically isolated from each other.

DCR losses of the inductor are based upon Inductor rms current square times inductor DCR. Inductor core losses are based upon inductor flux density, frequency of operation and core volume. Core vendors also provide curves that can be used to estimate core losses.

For ferrite cores, Steinmetz equation defines the core losses. $PL = K\beta^a (\frac{f}{10^6})^b (\frac{V_e}{1000})$ where frequency is in Khz, and core volume in cm

VI. OUTPUT CAPACITOR SELECTION

Output capacitor is selected based upon two critical criteria's, for example equivalent series resistance (esr) of the capacitor which along with the inductor ripple current will determine the output ripple voltage to meet the customer specifications.

Secondly the bulk capacitance, which along with the converter bandwidth determines the maximum overshoot and undershoots during transient conditions.

VII. SMALL SIGNAL MODEL OF BUCK CONVERTER

Once the power components have been specified, it is necessary to design a feedback compensator for the converter. The compensator will ensure that the output voltage remains at a fixed, stable value in spite of changes or perturbations in the input voltage and load current. This task is complicated by the fact that a dc-dc converter is a non-linear system, so an easy-to-understand mathematical description or dynamic model of the converter is not immediately evident. Such a model must first be derived, first by averaging the dc-dc converter to eliminate the effects of switching. This leaves a non-linear system, which can then be perturbed around an operating point, and then linearized to allow the use of well-understood linear system analysis.

The resulting dynamic model of the converter consists of a set of small-signal transfer functions that show how the variations of the input voltage and duty ratio affect the output

voltage of the converter. The feedback compensator is designed to stabilize the dynamic model directly or indirectly through the duty ratio to output voltage transfer function.

There are various analysis techniques to derive the small signal transfer function, most notably state-space averaging and PWM switch analysis.

In a converter operating in CCM mode switching ripple is small, so what we are interested in modelling the ac variation in the converter waveform. The model approach being discussed is applicable not only to buck converter but to any topology. Switching ripple in the inductor and capacitor waveforms are ignored by averaging over the switching period.

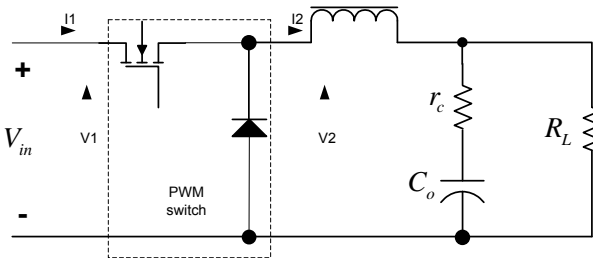


Fig 3 – Buck converter with PWM switch

We are interested in creating a model of the PWM switch [Ref 3]. The switch network terminals can be defined by two voltages (V1, V2) and two currents (I1, I2). Two of the four terminal can be taken as independent inputs to the switch and the remaining two are dependence. The choice of which terminal is classified as independent is arbitrary, as long as inputs can indeed be independent in the converter. We can draw the waveforms at V1, V2, I1 and I2 over a switching period. If we define V2 and I1 as dependent variables and V1 and I2 as independent variables and then express the dependent variables V2 and I1 as a function of independent variables V1, I2 and d duty cycle.

$$\langle v_2(t) \rangle_{T_s} = \langle v_1(t) \rangle_{T_s} \cdot d(t) \quad \langle i_1(t) \rangle_{T_s} = d(t) \cdot \langle i_2(t) \rangle$$

Next step we perturb and linearize the equations, where we assume average voltage consists of “dc” component and small signal “ac” variation around “dc” component.

$$V_2 + \hat{v}_2(t) = D(V_1 + \hat{v}_1(t)) + \hat{d}(t)V_1$$

$$I_1 + \hat{i}_1(t) = D(I_2 + \hat{i}_2(t)) + I_2 \hat{d}$$

Now the above equations can be expressed as shown below is equivalent model of PWM switch.

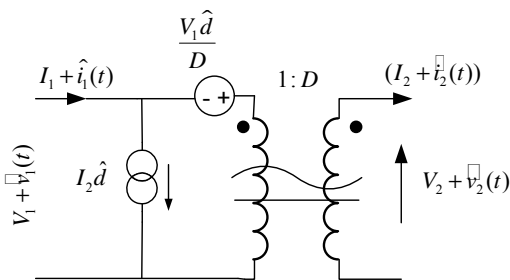


Fig 4 – PWM switch model

PWM switch model can be incorporated into the buck converter thus allowing us to analyze the complete circuit.

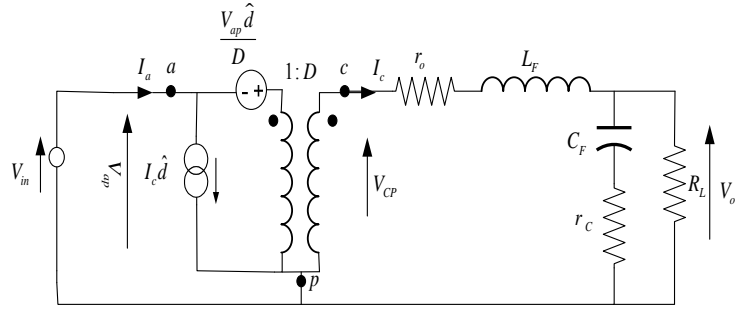


Fig 5 – Buck converter with PWM switch Model

For DC analysis we short the inductor and open the output capacitor and duty cycle \hat{d} is set to zero. This will give us $D=V_o/V_{in}$ dc gain. $V_{ap} = V_{in}$ & $V_{cp} = V_{out}$. For “ac” analysis we short the “DC” input source and analyse the circuit.

The duty ratio to output transfer function is the most important one, as it is utilized to design a feedback loop. It can be evaluated very simply as indicated below, where Z_L is the output inductor impedance and Z_x is the output capacitor in parallel with output load impedance.

$$\frac{\hat{v}_o}{\hat{v}_{cp}} = \frac{Z_x(s)}{Z_x(s) + Z_L(s)} \quad \frac{\hat{v}_{cp}}{\hat{d}}(s) = V_{in}$$

$$\frac{\hat{v}_o}{\hat{d}}(s) = \frac{\hat{v}_{cp}}{\hat{d}}(s) \cdot \frac{\hat{v}_o}{\hat{v}_{cp}}(s)$$

This is a very straight forward approach but can get fairly complicated to evaluate if multiple output capacitors with different impedances are involved.

An alternate method is to write the differential equation for voltage across the output inductor and current through the output capacitor, and then solve it using matrix methods. This allows us to use software like MathCAD to provide the final results.

$$L \frac{di_L}{dt} = \hat{i}_L(-r_o - Den) - Den \frac{V_c}{r_c} + V_{ap} \hat{d}$$

$$C \frac{dv}{dt} = \hat{i}_L \left(\frac{Den}{r_c} \right) + v_c \left(\frac{1}{r_c^2 Den} - \frac{1}{r_c} \right)$$

$$Den = \frac{R_L}{1 + \frac{R_L}{r_c}}$$

$$sX(s) = AX(s) + Bd(s)$$

$$sIX(s) = AX(s) + Bd(s)$$

$$(sI - A)x(s) = Bd(s)$$

$$(sI - A) \frac{x(s)}{d(s)} = B$$

Duty cycle to Output transfer function can be evaluated using Cramers rule as indicated below, where Δ refers to determinant of the matrix.

$$\frac{v_o(s)}{d(s)} = \frac{\Delta \left(\frac{v_o}{d} \right)}{\Delta}$$

Output LC filter is a low-pass filter used to average the switched waveform. The feedback compensator consisting of an error amplifier and a compensation network, is used to compensate the LC filter response and regulate the output voltage.

An intuitive way to look at the output LC is as follows. As frequency increases impedance of output capacitor decreases resulting in reduction in output voltage (open loop condition). Similarly, as frequency increases impedance of inductor increases, which tends to disconnect output from the input, each of these mechanisms resulting in with a slope of -20db/dec , this is referred to as a pole in the system. Thus one can see that the number of poles in the circuit is equal to the number of effective reactive elements. If two inductors are placed in series, it will perform as a single effective element and thus result in one pole, similarly if two capacitors are placed in parallel it will be an effective single capacitor and result in single pole. Output LC low pass filter will result in two pole response and depending upon damping or Q factor will result in peaking at the resonance frequency or (splitting the real poles as in the case of current mode control) instead of complex poles. Now as the frequency is increased, the output capacitor impedance will reduce and capacitor series resistor (esr) will tend to dominate. This will add a zero to the circuit. Thus Output LC filter gain performance can be visualized as shown below.

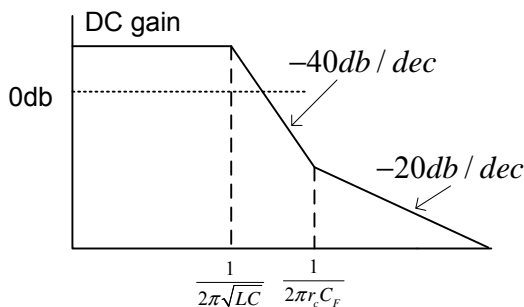


Fig 6 – Output LC gain response

VIII. CONTROL METHOD SELECTION

When high input to output ratio is required, which implies that low duty cycle or very narrow high side on-time pulses must be controlled. Duty cycle for buck converter is equal to V_{out}/V_{in} .

Various control methods in buck topology are used namely Voltage Mode (VM), Current Mode (CM), Hysteretic and Constant-On-Time (COT) control. Current mode control is the most favoured since it allows simple loop compensation, MOSFET switch protection due to inherent short circuit protection and its inherent line feed-forward compensation. Each approach has its pro's and con's.

Voltage Mode forces output voltage to be equal to reference voltage, requires additional circuitry for over current protection.

Hysteretic controllers respond quickly to load transients but its operating frequency is not constant with line and load variations.

COT also responds more quickly to load transients but will still have some variations in its operating frequency.

Current Mode control on the other hand has its issues also namely [Ref 7].

1. On-time of conventional current mode controller is limited by current measurement delays and the leading edge spike of the current sense signal. When the buck FET turns on and the diode turns-off, a large reverse recovery current flows. This current can trip the PWM comparator. Additional filtering or leading edge blanking is necessary to prevent premature tripping of the PWM.
2. Conventional current mode is also susceptible to noise on the current signal thus limiting its ability to process narrow pulses.
3. As duty-cycle approaches 50% current mode exhibits sub-harmonic oscillations. Thus a fixed ramp signal (slope compensation) is added to the current ramp signal to address the issue.

Current mode control also have its advantages, which make it very popular in the industry.

4. Current mode control is a single pole system. Due to current loop, the poles of output LC filter split into two real poles, thus resulting in output inductor pole to be at much higher frequency. The current loop forces the inductor to act as constant current source. Thus loop remains as a single pole system regardless of the conduction mode.
5. By clamping the error amplifier, peak current limiting function can be implemented.
6. It also provides ability to current share multiple module.

An improved version of current mode control “Emulated peak Current mode controller” LM3495 exhibits the advantages of current mode control, without the noise susceptibility problems often encountered from diode reverse recovery current, ringing on the switch node and propagation delays.

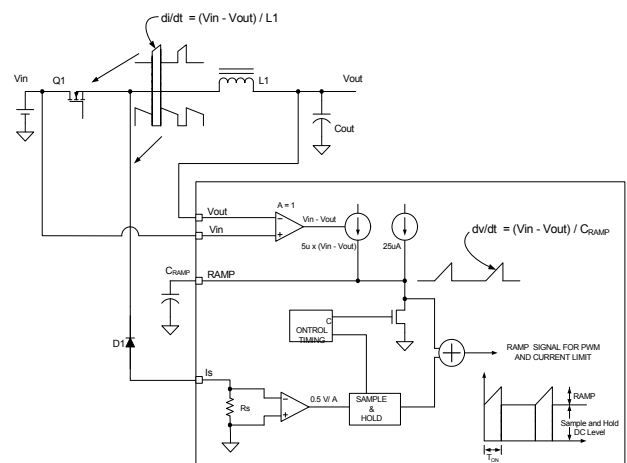


Fig 7 – LM3495 Emulated CMC buck converter, Ref [7]

Figure 7 shows a buck converter consisting of Q1, D1, L1 and Cout. For synchronous buck converter diode can be replaced by a MOSFET. LM3495 creates a signal that accurately represents the current thru the buck switch Q1 without making a direct measurement. We can emulate the buck switch current by having a pedestal and a ramp. This is achieved as follows: by taking a sample and hold measurement of the diode current (by using a sense resistor) just before the turn-on of buck switch. The 2nd part of the buck switch current is created with a current source proportional to $V_{in}-V_{out}$ and a capacitor C_ramp. Value of C_ramp can be selected to set the capacitor voltage slope that is proportional to the inductor current slope.

For duty cycles above 50%, current mode control is prone to sub harmonic oscillations. This is addressed by adding a fixed slope to the current sense ramp.

An added benefit of ECM is its “look-ahead current limiting”. Inductor current is measured near the end of diode conduction period and prior to turning on the buck switch. During extreme overload conditions, if the inductor current does not decay below the current limit threshold, buck switch will skip cycles to prevent current runaway condition.

Hysteretic regulator is the simplest of all the controllers. In this control method, the switch is turned on when the output voltage is below a reference and turns off the switch, when the output voltage rises above the reference voltage. The output ripple is a function of upper and lower reference threshold. One major disadvantage of this approach is very large variation of switching frequency as the input voltage varies.

Constant on-Time (COT) controller is a variation of hysteretic controller that reduces the variation of switching frequency as the input voltage varies. In this approach, a one-shot timer is inserted in the signal path. The period of one-shot is inversely proportional to the input voltage. On-time programming requires only one resistor connected to V_{in} . Upper threshold is eliminated and replaced by the programmed on-time. Lower threshold still requires the output voltage to have enough ripple to be distinguish the falling output turn-on point. The regulator comparator looks at the output voltage thru feedback divider. This approach will work properly, as long as output capacitor has enough esr at the switching frequency. It regulates the bottom of the output ripple, and when output decays below the bottom level, a programmed on-time is initiated, which forces the output higher than the feedback pin voltage.

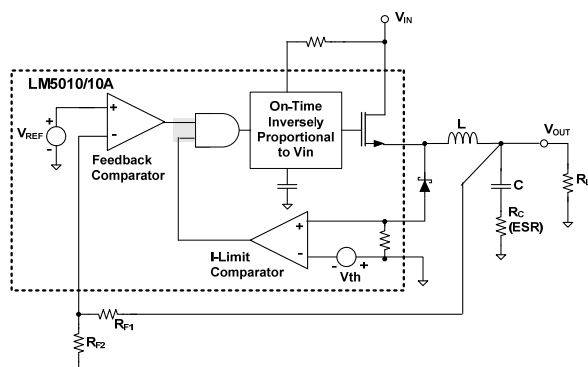


Fig 8 – COT buck converter using LM5010

In order to ensure minimum output ripple a variation that incorporates two capacitors and one resistor is highlighted. V_{out} is at “ac” ground, Switch pin switches between V_{in} and “ac” Gnd. Ripple is generated by RA and CA. Triangular waveform resulting at RA/CA junction is ac coupled to the FB pin. This configuration makes the design independent of output capacitor esr.

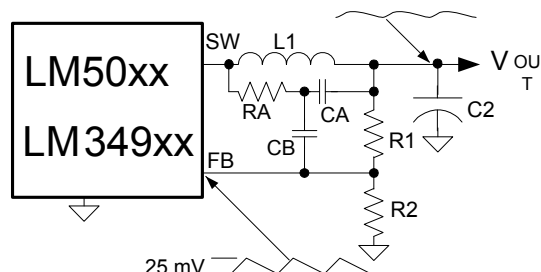


Fig 9 – COT converter with reduced output ripple

In summary, we have reviewed the synchronous buck converter and developed a small signal model that can be used to analyze the circuit. Also reviewed an intuitive look at the Output LC filter, reviewed the MOSFET switching behaviour and criteria’s used in selecting high side and low side MOSFETs. Output inductor losses and issues relating to it. Finally, various control architectures are reviewed for high step-down ratio converters.

Reference: [1],[3] - [6],[8] - [10] for further reading.

IX. REFERENCES

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