3D IC Pixel Electronics- the Next Challenge

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Abstract

There is no question that 3D integrated circuit design will play an important role in the continuing development of high performance integrated circuits. This paper will provide a brief introduction to the markets for 3D integrated circuits and the technologies that are used, followed by a review of 3D activities in High Energy Physics (HEP). The paper will review the first 3D chip for HEP and conclude with discussion of a collaborative effort to use a commercial vendor to fabricate 3D ICs as a path forward to meet the next challenge for electronics designers in HEP .

I. Overview of 3D/Vertical Integration

A. Introduction

The just released Handbook of 3D Integration defines 3D integration as "the integration of thinned and bonded silicon integrated circuits with vertical interconnects between IC layers". [1] This book is an excellent reference for those wanting to understand the fabrication principles for 3D as well as the approaches various organizations are taking to develop vertical integration.

Vertical integration is now in a position to allow significant improvements to those drivers that are critical to the semiconductor industry. More specifically, in the right application, 3D can provide 1) better electrical performance, 2) lower power consumption, 3) higher functionality, 4) improved form factor, 5) mixed technologies, and 6) lower cost.

B. Industrial Markets for 3D

There are a number of markets that are studying 3D. All major memory manufactures are working on 3D memory stacks. Significant cost reduction can be expected for large memory devices. The memory cost can be considerably less than going to a deeper technology node.

Pixel arrays with sensors and readout are well suited to 3D integration since signal processing can be placed close to the sensor. Current 2D approaches cannot handle the data rate needed for high speed imaging applications.

Microprocessors represent another market. A major bottleneck is access time between the memory and CPU. Memory caches are used as an interface but they require a significant amount of expensive chip real estate. Initial applications for 3D will use Logic to Logic stacking and Logic to Memory stacking.

Finally, in 2D FPGAs, wire delays are an inherent problem. 3D integration can improve the performance by moving the programmable interconnect circuitry from the logic block layer and placing it on a separate tier.

C. HEP Applications for 3D

The industrial markets are large and there is little HEP can do to influence the paths that they take toward vertical integration. However, there are already two areas where HEP can stand to benefit from the current state of the art.

The first is in the area of 3D pixel arrays. There are already descriptions of working 3D circuits with a sensor layer and two layers of electronics [2], [3]. In addition, Fermilab has already built a circuit with 3 layers of electronics where the total thickness of the electronics portion is only 22 microns [4]. The Fermilab circuit was designed as a demonstrator for the International Linear Collider (ILC). This circuit will be discussed in more detail later on.

The other area of interest for HEP is 3D bonding technology as a replacement for bump bonds in hybrid circuits. Fermilab worked with RTI International to develop CuSn eutectic bonding with small interconnect pillars for fine pitch bonding [5]. Initial tests showed the CuSn bonds to be stronger than conventional PbSn solder connections. Figure 1 show these pillars on a 50 micron pitch and a cross section of one of the connections.

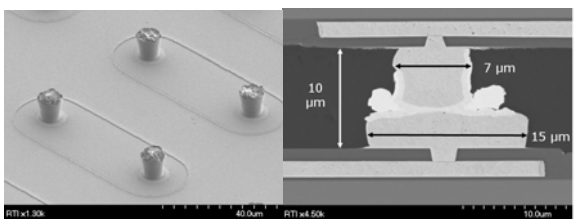

Figure 1: (l) 7 micron diameter pillars on 50 micron pitch, (r) cross section of solder connection showing height of connection.

If post processing such as thinning a part after bonding is required, the percentage of bonded surface area needed to hold the parts together can be significant. Because of the 10

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micron bond thickness, the bonded area may represent too much mass for some applications.

Another option of interest is the Direct Bond Interconnect (DBI) developed by Ziptronix. Minimal mass is required for bonding with the DBI process. Bond pitches as small as 3 microns have been demonstrated. Figure 2 shows 25 pixel sensors bonded to a Fermilab BTEV pixel ROIC wafer using DBI. After the chip to wafer bonding, the sensors were thinned to 100 microns. Due to the large surface bonding area associated with the DBI process there was no damage to the sensors during the thinning process.

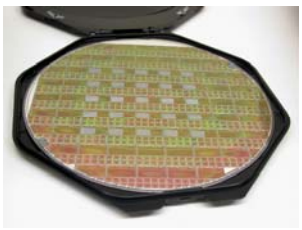

Figure 2: Sensors bonded to ROIC using DBI process

A third option, called CuCu bonding, which also provides a low mass interconnect, is being pursued by Fermilab. A CuCu bond uses a very thin copper bond pad on each surface. If post processing such as thinning is needed, a relatively large part of the surface area will need to be bonded just like a CuSn bond. The advantage to CuCu bonds is that the thickness of the bond material is so small that it does not add significantly to the mass of the circuit. This process is used by Tezzaron and it will be described later in this paper.

II. Basic Principles for 3D

There are four key technologies needed for 3D integration, 1) via formation, 2) bonding, 3) precision alignment, and 4) thinning.

There are two main approaches to via fabrication. One is called "via first" and the other is called "via last". In the "via first" process, the vias are an integral part of the wafer fabrication process. Thus the vias are imbedded in the wafer at the foundry. The vias can be fabricated either before or after the transistors are formed.

In the "via last" process, the vias are added to the wafers after the front end of line (FEOL) and back end of line processing (BEOL) has been completed. These vias are often added by a third party vendor.

The trend for low cost vias seems to be moving toward the "via first" process. Later in this paper there are examples of the "via first" and the "via last" processes.

The via formation processes are different in SOI CMOS and bulk CMOS processes. In CMOS the Bosch process is usually used to form vias. These vias need to be passivated before filling with metal to avoid shorts between all the vias. In the SOI process, a different etch process must used to form the via but no passivation is needed before filling since the vias are already in an insulator.

There are five bonding options that are commonly used for 3D fabrication. These are all shown in figure 3. One bonding approach uses a polymer adhesive (typically BCB) to form a uniform bond over the entire surface. A second approach uses an oxide bond where an oxide covers most of the surface area to be bonded. The oxide surfaces are specially prepared and brought together to form an exceptionally strong silicon dioxide to silicon dioxide bond. With both the adhesive bond and the oxide bond, vias are formed after bonding to form the electrical connections between the parts being bonded. CuSn eutectic bonds are form by placing copper on two mating surfaces and then placing a small amount of tin on the copper on one of the surfaces. The surfaces are then brought together and heated to form a high temperature eutectic bond. Typically the copper is 5 microns thick on each surface. With CuCu thermo compression bonds, thin copper pads are placed on each surface (normally the pads are a fraction of a micron thick). After careful cleaning, the surface are mated and heated to form the bond. The final option, called DBI, is a combination of two ideas. Oxide surfaces are prepared with small imbedded metal contacts that have high thermal coefficient of expansion. When the surfaces are brought together an oxide bond is immediately formed. After some time, the assembly is heated and the high expansion metal forms a compression bond. With the CuSn eutectic bond, the Cu thermo compression bond, and the DBI processes, both the mechanical and electrical connections are formed at the same time. Fermilab has been working with different vendors on options b, c, d, and e shown in figure 3.

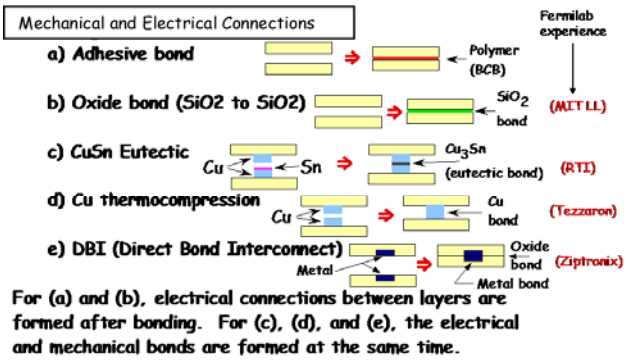

Figure 3 – bonding options

Currently wafer to wafer 3 sigma bonding alignment is better than 1 micron. Typically vias have an aspect ratio of about 8 to 1. Therefore it is important to thin the wafers as much as possible in order to reduce the area needed for vias. Figure 4 show a very thin wafer.

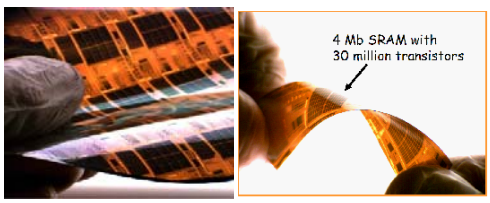

Figure 3: 6 inch wafer thinned to 6 microns and mounted to 3 mil kapton (MIT LL)

III. Activity in HEP

Fermilab submitted the first 3D integrated circuit for HEP to MIT Lincoln Labs in October of 2006. In November of 2007 there was a meeting sponsored by CNRS/IN2P3 in

France called the 3D Integration Technologies Perspectives. Closely following this meeting there was another workshop in April 2008 sponsored by the Max Planck Institute called Vertical Integration Technologies for HEP and Imaging sensors. As a result of these activities new programs are developing. In Italy, the Ministry of Research has funded a 2 year program on 2D MAPS and Vertically Integrated Sensors that will focus on device and technology investigations rather than specific experiments. Another Italian effort is the INFN proposal for Pixel Systems for Thin Charged Particle Trackers Based on Vertical Integration Technologies. This 3 year program will focus on experiments like Super B and the ILC. After the meeting in France funding was approved for several French labs to develop vertically integrated circuits. Applications for the ILC, SHLC and imaging are expected.

At Fermilab a second 3D chip will be submitted to MIT LL in October 2008. In addition, Fermilab is forming an international 3D HEP collaboration for a multi project wafer run to develop vertically integrated circuits through Tezzaron. The run will have two stacked circuits with a deep N-well option. Up to 10 fully integrated 3D wafers will be fabricated in a 130 nm process. Submission is targeted for early 2009. Thus it is clear that interest for 3D has grown within the HEP community.

A. Description of first 3D Circuit for HEP

The first 3D chip designed for HEP was called the VIP1 (Vertically Integrated Pixel). It was a demonstrator chip for the ILC vertex detector. The chip was designed in the MIT Lincoln Labs 0.18 micron SOI process and had three tiers of stacked electronics. Details of the VIP1 circuit design were presented at the 12th LHC electronics workshop [6] and are not repeated here. The chip included all the major features needed for a vertex detector chip:

Readout between ILC bunch trains

High speed data sparsification

Analog outputs from each pixel for improved resolution

High resolution digital and analog time stamping

Test input for every pixel

20 micron pixels in a 4096 pixel array.

A block diagram of the chip is shown in figure 5.

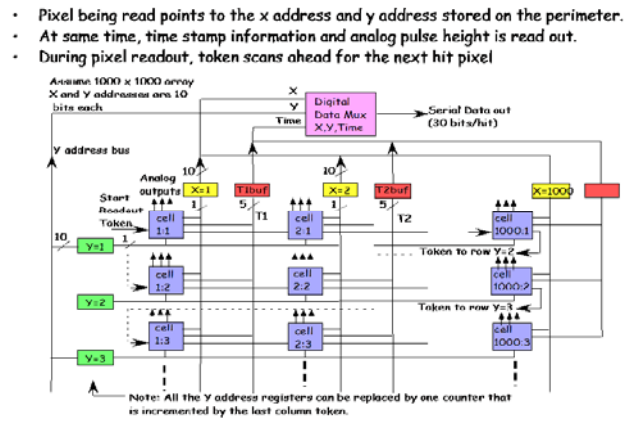

Figure 5 – Block diagram of 1 MPix VIP1 chip

Most time stamping circuits designed to date for the ILC vertex detector are limited to 6-20 time stamps per msec. The digital time stamp in VIP1 uses a 5 bit Gray code counter that provides 32 time stamps/msec and it is easily expandable. Figure 6 shows both the digital and analog time stamp circuits. The digital time stamp circuit has a slow counter on the perimeter which counts up during the 1 msec bunch train. When a hit occurs, the current state of the counter is latched in the hit pixel for read out at a later time. The analog time stamp has a slow ramp generator on the perimeter that rises 1 volt during the beam train. When a hit occurs, the analog value of the ramp is latched in the pixel for read out. The digital and analog time stamps can be setup so that the digital time stamp provides a coarse 5 bit time stamp and the analog time stamp provides additional bits for higher resolution.

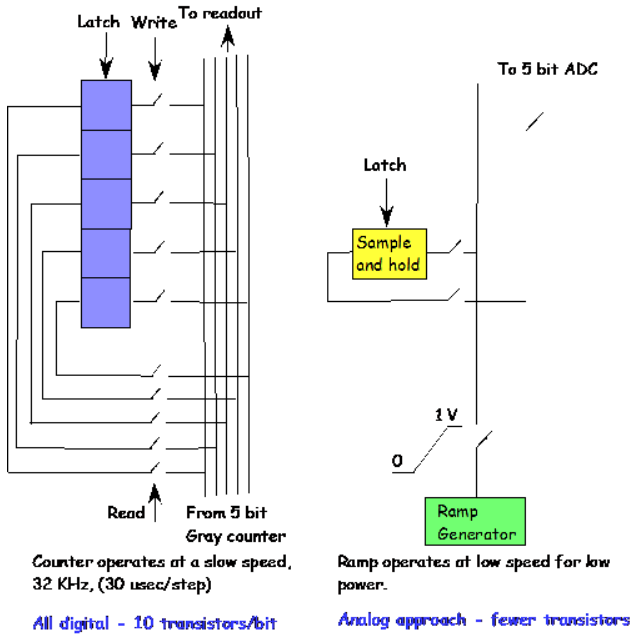

Figure 6 – VIP1 digital and analog time stamps

Figure 7 shows a single cell block diagram of the VIP1 and figure 8 shows how the pixel is mapped into a 3D structure. There are 3 main parts: the analog front end with a test input and double correlated sampling, a pixel sparsification section with hit look ahead capability, and the time stamp section.

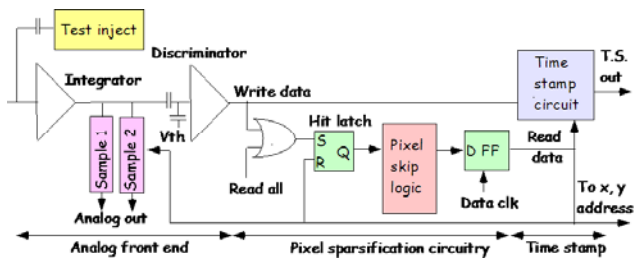

Figure 7 – Simplified VIP1 pixel cell block diagram

The MIT LL process used to build the VIP chip is a "via last" process wherein the vias are added after wafer fabrication and wafer to wafer oxide bonding is completed. The total height of the electronics in the 3 wafer stack is only 22 microns as shown in figure 8.

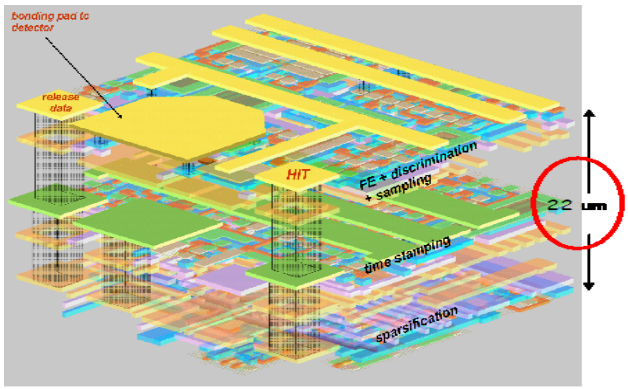

Figure 8 – 3D circuit diagram and 3D layout of pixel cell

B. *Test results of first 3D chip [8]*

The basic functionality of the VIP1 has been demonstrated through the following series of tests.

Full sparsified data readout

Successful operation of the token passing scheme

Operation of the digital and analog time stamp circuits

Threshold scan

Input test charge scan

Fixed pattern and temporal noise measurements

At the present time, no problems have been found related the 3D interconnects. On the other hand, the chip performance was severely compromised by poor transistor models and low yield. It should be pointed out that the same readout architecture has been demonstrated in a 2D MAPS device fabricated in the ST 130 nm process [7].

Figure 9 shows hits pixels in the full 64 x 64 array as a function of threshold. The readout is done using the sparsified data readout scheme.

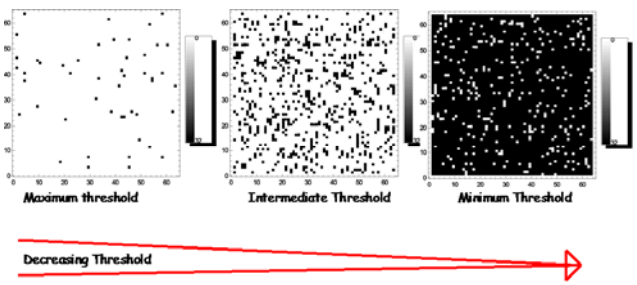

Figure 9 – Hit pixels versus threshold

Pixel to pixel threshold dispersion is shown in figure 10. The plots were taken by setting the common pixel threshold at increasing levels (no charge injection) and reading out all pixels over threshold using the data sparsification scheme.

The left hand plot in figure 10 was made with the integrator reset and shows threshold dispersion with a sigma of 25 e. The right hand plot was made with the integrator released and with the discriminator auto zeroed and shows a dispersion of 75 e. The increase in dispersion is thought to be due to internal coupling problems.

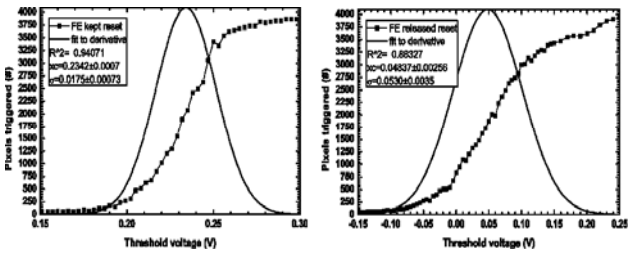

Figure 10 – Pixels triggered versus threshold voltage

Another test was performed injecting a test charge into 119 pixels to simulate a hit pixel pattern. The left hand side of figure 11 shows the preselected hit pattern. The right hand side shows the pixel pattern read out using the standard data full sparsification scan. Although the results are not ideal, they demonstrate successful operation of the test inputs.

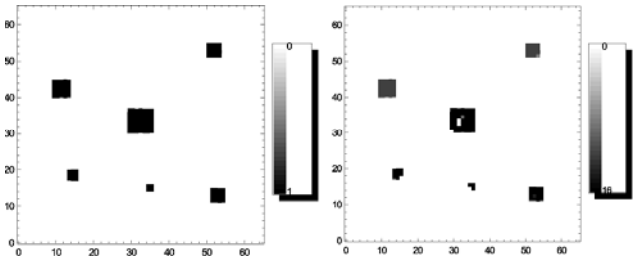

Figure 11 – Array hit input (l) and array hit output (r)

The analog signal response from the pixels in the 119 pixel test pattern was shown to be reasonably linear as seen in figure 12. As the level of the test charge through the test capacitor (0.2fF) was increased more pixels exceeded the threshold up to 119. The plot shows the mean analog signal level of those pixels exceeding the threshold voltage. The superimposed line is an indication of the linearity. There is no signal at low input voltages due to the small size of the injection capacitor.

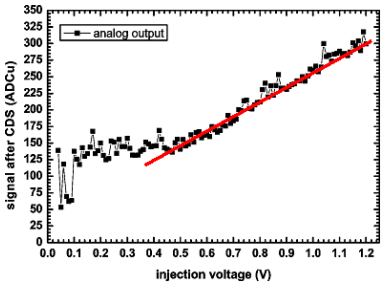

Figure 12 – Mean analog output voltage versus injected voltage

The digital time stamp circuit was shown to work but had a significant dependence on the power supply voltage. In a test, the 119 pixel hit pattern was injected at different times and the time stamp was read out. At a supply voltage of 1.4 V, the time stamp was correct for 118 of the 119 pixels. The analog time stamp, while working, gave poor results due to high leakage current in the sample and hold circuit.

A new improved version of the chip is being prepared for submission. The goal of the new submission is for improved yield and performance at the expense of a larger pixel size.

IV. A Path to the Future

Development of 3D integrated circuits is a challenge for a number of reasons. Depending on the approach taken, the cost can be high. Because most 3D processing is done at the wafer level, access to full wafers is needed. Finally the choice of vendors for small customers is very limited at this time. Fortunately Fermilab has found a vendor, Tezzaron, willing to do a multi project 3D wafer run. The run cost is reasonable.

As a leader in 3D technology, Tezzaron has built 3D devices for imaging, memory stacking, FPGAs, and microprocessors. Currently Tezzaron is gearing up to produce 10,000 3D wafers/month in 18 months. The 3D chips will include 2, 3, and 5 layer stacks of memories from 512Mb to 4 Gb. The wafers will be fabricated by Chartered in Singapore where the 3D assembly is completed by Tezzaron. The Tezzaron 3D assembly process is expected to be in 1 to 3 more foundries by the end of the year. The advantages of using Tezzaron include: existing rules for vias and bonding contacts, low cost, reasonable turnaround, one-stop shopping for wafer fabrication, via formation, thinning, and bonding. Fermilab has organized a collaboration of 6 French labs and 6 Italian labs to contribute to a MPW run at Tezzaron.

Chartered is one of the world's top semiconductor foundries with an extensive line of CMOS and SOI processes down to 45 nm. Tezzaron has chosen the 130 nm CMOS process for 3D integration. Chartered has fabricated nearly 1 million 8 inch wafers in the 130 nm process and data demonstrates consistent high yield. Chartered is working to extend through silicon via (TSV) processes to 300 mm wafers and 45 nm technology. There is a full set of commercial tools to support the 130 nm process. The 130 nm process is well suited to analog circuit design offering deep N-wells, MiM capacitors, and multiple threshold voltage transistors.

The Tezzaron 3D process is a "via first process where TSVs (super contacts) are formed after FEOL processing as shown in figure 13. The vias are only 6 microns deep. Figure 14 (l) shows the bonding of two identical wafers using a CuCu bond in a face to face configuration. Figure 14 (r) shows the top wafer thinned to 12 microns to expose the vias and metallization added for bump bonds or wire bonds

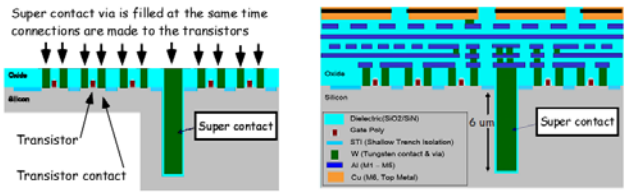

Figure 13 – (l) FEOL processing with connections to transistors and filled vias, (r) wafer with completed BEOL processing.

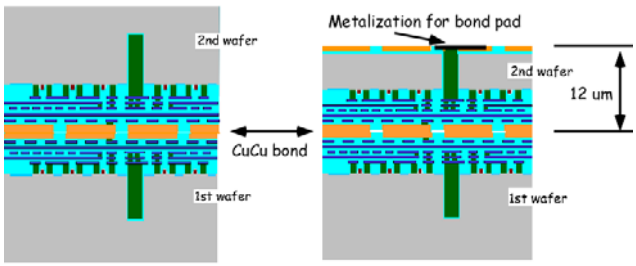

Figure 14 – (l) face to face bond, (r) completed wafer stack

The Fermilab 3D MPW run will use a face to face bond as shown in Figure 14 to form a two wafer stack. To reduce mask costs, a single set of masks will include both the top and bottom circuits. For devices that do not have an integrated sensor, bond pads will be added to the top wafer for bonding to sensors at a later time using the Ziptronix DBI process.

The 3D collaboration expects to make a MPW submission in the first part of 2009. Submissions from Italy, France, and Fermilab will include projects for the ILC, SLHC and Super B. The cost of fabricating 25 eight inch wafers in the 130nm process and complete 3D assembly should be under $300 K.

V. Conclusion

New technologies have always presented challenges to HEP. Success with new technologies in HEP has often led to dramatic advances. Industry is making rapid progress in developing 3D integrated circuits. HEP is beginning to respond with new initiatives to explore this technology. Fermilab has been working with different 3D technologies for over 2 years and has now begun a collaboration with 12 international laboratories in France and Italy to use the Tezzaron 3D process to develop circuits for ILC, SLHC, and related applications. We believe that the collaboration will provide an excellent path forward for development of 3D integrated circuits to help HEP meet the 3D challenge.

VI. References

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