

# Evaluation of Multi-Gbps Optical Transceivers for Use in Future HEP Experiments

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## Abstract

Future experiments at the European Organization for Nuclear Research (CERN) will increase the demand for high-bandwidth optical links. Custom developments for deployment within the detector volumes might be based on commercially available optical transceivers (TRxs).

We present our evaluation of Commercial Off-the-Shelf (COTS) multi-Gbps optical TRxs. This serves as the basis to evaluate the performance of the future Versatile Transceiver (VTRx) that is being developed at CERN in the context of the Versatile Link project. We describe the devices evaluated, the experimental set-up for parametric testing, and our analysis of the performance data.

## I. INTRODUCTION

High Energy Physics (HEP) experiments, such as the ones currently undergoing commissioning at the Large Hadron Collider (LHC), require tens of thousands of optical links each in order to extract raw data from the detector and to distribute clock and control data to the front-end electronics. An upgrade of the current LHC (super LHC or SLHC), planned for 2016-18, is expected to increase the luminosity by an order of magnitude to  $10^{35}/\text{cm}^2/\text{s}$ , which implies more data to be transmitted (assuming more complex detector systems) and higher radiation doses. Since the optical links are also required to have low power dissipation and to reduce the mass inside the detector, the solution is to increase the bandwidth of each individual link.

Optical Links for SLHC are being developed in collaboration between CERN and other institutes [1]. This effort is divided into the GigaBit Transceiver (GBT) project and the Versatile Link (VL) project. The former covers the

design of radiation-hard Application Specific Integrated Circuits (ASICs) and the implementation of the custom GBT protocol in an FPGA. The latter covers the system architectures and the basic building blocks required for the implementation of future single-mode (SM) and multi-mode (MM) optical links across the various SLHC experiments. A system outline is shown in Figure 1.

One of the main building blocks is the Versatile TRx module for on-detector deployment that will be available in both 850nm and 1310nm versions. The VTRx modules must operate in the innermost regions of a detector, where the magnetic field can reach up to 4T and the radiation field will be dominated by particles with energies around 300MeV at fluxes of maximum  $10^8$  particles/cm<sup>2</sup>/s [2]. In addition, the VTRx modules are required to work at multi-Gbps speeds, to have small size/mass and dissipate low power. To build the VTRx on the packaging know-how of the optoelectronics industry, the VTRx will be based on commercially available multi-Gbps optical TRxs by customizing only those aspects that are absolutely necessary.

To aid the selection of a TRx type for VTRx customization and to be able to evaluate and qualify the VTRx prototype modules we have developed test methods based on commercially available parts. We have set up test equipment, developed software tools and specified the evaluation criteria and test procedures. In the process, we have established performance benchmarks to which the VTRx modules can be compared.

This paper is structured as follows: Section II describes the parts that were evaluated. The test set-up and the metrics are the focus of section III. Section IV deals with the analysis of the performance data. Section V details the main conclusions of this work.

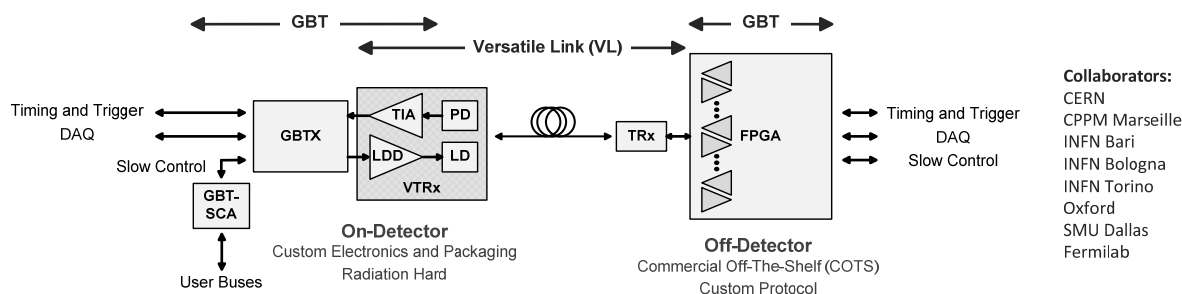


Figure 1: Radiation-Hard Optical Link for Experiments system outline.

## II. DEVICES UNDER TEST

There are several families of commercial optical TRxs that target telecom and datacom applications. The bitrates of some of the standards are shown in Figure 2.

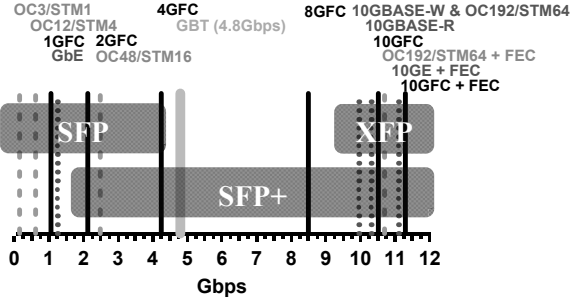


Figure 2: Selected TRx families and their corresponding bitrates.

Since the GBT protocol proposes a single lane running at a non-standard 4.8Gbps, there are only a few families of TRx modules that could be used for VTRx customization. Taking dimensions and power dissipation into consideration, we decided to evaluate three families: Small Form Factor Pluggable (SFP), Enhanced SFP (SFP+) and 10 Gigabit SFP (XFP). These module types are hot-pluggable serial-to-serial data-agnostic multirate optical TRxs used to implement SM or MM links. A picture of the modules is shown in Figure 3.

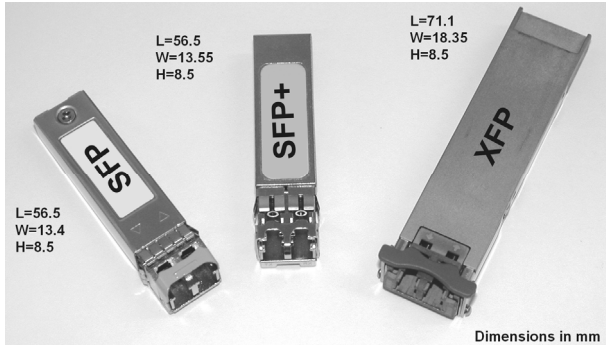


Figure 3: Three modules from the selected TRx families.

The maximum power dissipation found in SFP modules is 1.0W and the SFP+ specification allows for two power levels: up to 1.0W and up to 1.5W. Both the SFP and the SFP+ require the host board to provide a +3.3V supply. XFP modules must meet one of four power levels: up to 1.5W, up to 2.5W, up to 3.5W and higher than 3.5W. The XFP specification requires the host board to provide three supplies: +1.8V, +3.3V and +5V and allows for an optional -5.2V.

Table 1: List of evaluated transceivers and their main characteristics.

Device #	TRx Type	Wavelength [nm]	Max Bitrate [Gbps]	LD/PD type	Applications
1	SFP	850	4.25	VCSEL/PIN	1/2/4GFC; 1000BASE-SX
2	SFP	1310	4.25	VCSEL/PIN	1/2/4GFC; 1000BASE-LX10
3 and 4	SFP+	850	10.5	VCSEL/PIN	2/4/8/10GFC; 10GBASE-SR
5 and 6	SFP+	1310	10.5	DFB/PIN	2/4/8/10GFC; 10GBASE-LR
7	XFP	1310	10.3	DFB/PIN	10GBASE-LR/LW
8 to 12	SFP+	1310	10	VCSEL/PIN	Prototype for 10Gbps over SM fiber

The SFP+ SFF-8431 [3] specification is an expansion of the original SFP INF-8074i [4] specification plus the SFF-8472 [5] specification for Digital Optical Monitoring (DOM). As a consequence, both modules types have the same basic components: the Transmitter (Tx) has a Laser Diode Driver (LDD) and a Transmitter Optical Sub-Assembly (TOSA); the Receiver (Rx) has a Receiver Optical Sub-Assembly (ROSA) and a post-amplifier (AMP). The TOSA includes a Laser Diode (LD) and a monitor photodiode; the ROSA includes a Photodiode (PD) and a Transimpedance Amplifier (TIA). There is also a microcontroller and a memory inside the module for serial ID, Digital Optical Monitoring (DOM) and to control the module operation. The block diagram of an SFP/SFP+ module is shown in Figure 4.

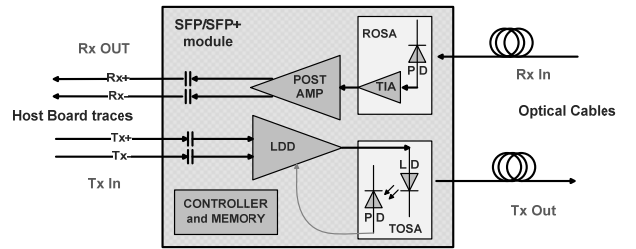


Figure 4: Block diagram of an SFP/SFP+.

The XFP [6] differs from the SFP/SFP+ by requiring a signal conditioner – Clock and Data Recovery unit (CDR) – in both Tx and Rx paths which resamples the data and resets the jitter, but also restricts the bitrates. The signal conditioner in the Rx path may include an amplifier to reduce the number of Integrated Circuits (ICs). The Serializer/Deserializer (SerDes) must be on the host board for all three modules.

During the course of this work we evaluated twelve commercial TRx modules. The devices and their main characteristics are shown in Table 1. The receivers of these TRx modules are all PIN-based and the 850nm semiconductor lasers are VCSELs. The 1310nm semiconductor lasers are either Distributed Feedback (DFB) diodes or VCSEL diodes.

## III. TEST SET-UP AND PERFORMANCE METRICS

To evaluate an optical TRx we must collect a set of metrics capable of quantifying the performance of its Tx and Rx parts [7]. We should also measure the power dissipation of the entire TRx module. Thus, the evaluation of an optical TRx module was divided in three parts: Tx performance, Rx performance and TRx power dissipation.

For each of the three TRx types we used a specific testboard in which a module is plugged. A picture of a testboard used for SFP+ modules is shown in Figure 5.

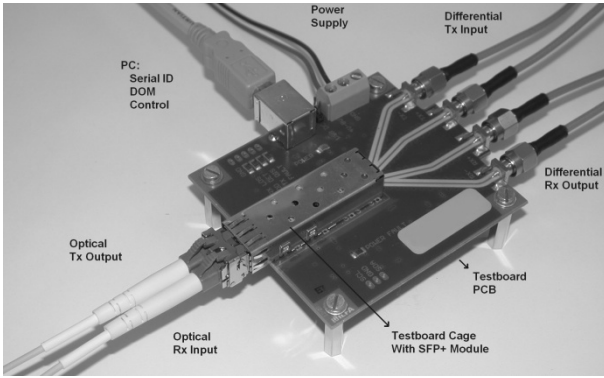


Figure 5: SFP+ testboard with TRx module and cables.

### A. Tx Evaluation

When evaluating the performance of an optical Tx we are interested in the characteristics of its optical output signal. For the purpose of our study we focused on power levels and general waveform characteristics. This information can be extracted from the Tx optical eye diagram using Set-up A shown in Figure 8.

The clock synthesizer is a Centellax TG1C1-A, the pattern generator is a Centellax TG2P1A and the scope is a LeCroy SDA100G with an SO-10 optical sampling module. A PRBS7 pattern whose characteristics are known is provided to the Tx input via the testboard and the Tx output is then measured by the sampling scope. No signal is provided to the Rx input and its output is terminated in the testboard.

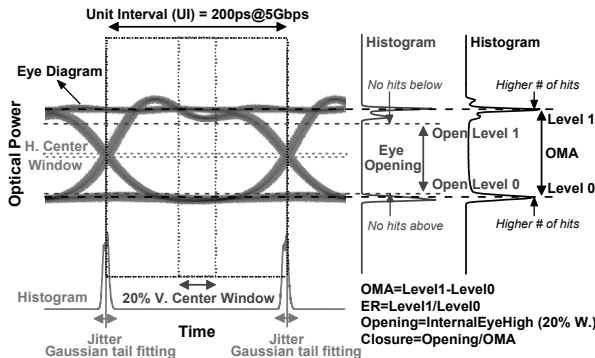


Figure 6: Tx eye diagram and definition of selected measurements.

We wrote a LabVIEW program that controls the instrumentation and automates the data acquisition. It runs through a list of bitrates (from 0.5Gbps to 12.5Gbps) and saves the performance data. This comprises the raw eye diagram, the jitter bathtub curve [8] and the values of various measurements (including rise/fall times and jitter). We then process the eye diagram to extract a few additional

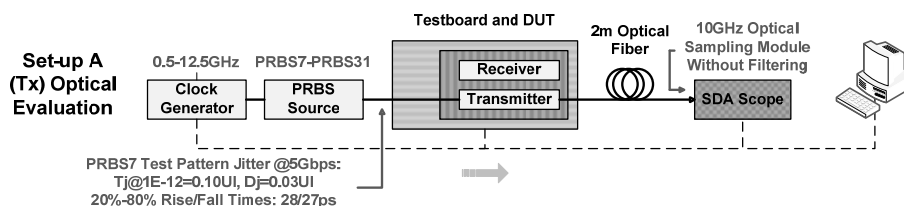


Figure 8: Set-up to evaluate the Tx part of a TRx module.

measurements: average power, OMA, ER and vertical eye closure in the 20% center window. The details are shown in Figure 6.

In Table 2 we propose a Tx performance specification for the module operation at 5Gbps, which is slightly faster than the current GBT protocol (4.8Gbps). It is based on the 4G Fibre Channel (4GFC) [9] specification with some values adjusted to the higher bitrate. The Tx maximum jitter is the 4GFC Tx jitter budget, not including the jitter of our test set-up.

Table 2: Tx specification proposal for 5Gbps operation.

#	Spec.	Min	Max	Unit	Notes
1	OMA	300		$\mu W$	
2	ER	3		dB	
3	Eye Closure	60		%	of OMA
4	Rise Time		65	ps	20%-80%
5	Fall Time		65	ps	20%-80%
6	Total Jitter		0.25	UI	@BER= $10^{-12}$
7	Det. Jitter		0.12	UI	
8	Tx Mask M.	0		%	Figure 7

Point 8 of the specification in Table 2 is a mask margin test. The Tx relative mask defines an area that the optical eye diagram must not cross and is used to keep the overshoot/undershoot/ringing under control. The mask in Figure 7 is based in the 4GFC Tx mask with jitter and slope adjusted to the previous specification and to the jitter of our test set-up. The arrows define the expansion of the mask from 0 to 100% to quantify the mask margin.

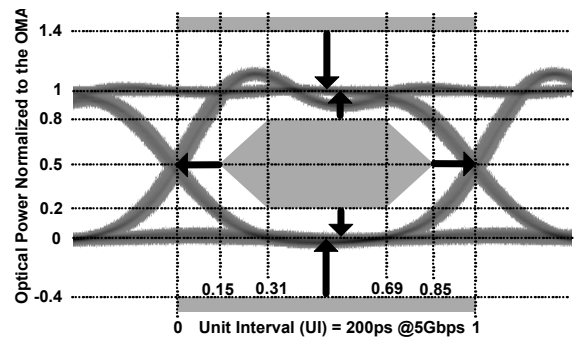


Figure 7: Tx eye diagram and Tx mask definition.

### B. Rx Evaluation

To evaluate the performance of an optical Rx we measure the Bit Error Rate (BER) curve and extract the Rx sensitivity (minimum OMA for a BER of  $10^{-12}$ ). We also measure the electrical swing and the jitter of the Rx output. Figure 9 shows the two set-ups required for this evaluation.

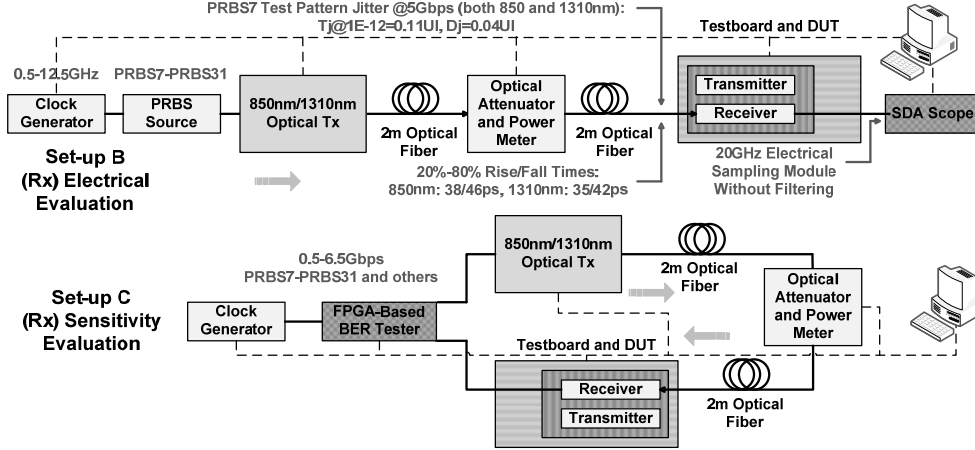


Figure 9: Set-ups used to evaluate the Rx part of a TRx module.

The electrical signal from the PRBS generator or the FPGA is first converted to optical by a reference Tx and then its power is controlled and measured by an Optical Level Attenuator (OLA) and a Power Meter (PM). The attenuated signal is then fed to the Rx input and its electrical output is finally sampled by a LeCroy SDA100G with an electrical module (ST-20) or compared with the original electrical signal generated by the FPGA.

To automate Set-up B we wrote a LabVIEW program that runs through a list of bitrates/attenuations and stores the following data: Optical input power, raw eye diagram and jitter bathtub of the electrical output and several additional measurements (including the jitter components). In Set-up C the BERT was implemented on an FPGA board from Xilinx using their reference design. A LabVIEW program automates this set-up by running through several attenuations and saving the BER data.

In Table 3 we propose a specification for the Rx operation at 5Gbps. The Rx maximum jitter is the 4GFC Rx jitter budget. The OMA of the input signal for the jitter measurement and the Rx sensitivity are mid values between the 4GFC requirements for MM and SM links.

Table 3: Rx specification proposal for 5Gbps operation.

#	Spec.	Min	Max	Unit	Notes
9	Total Jitter		0.26	UI	@BER=10 <sup>-12</sup> , OMA=90 μW
10	Det. Jitter		0.11	UI	OMA=90 μW
11	Rx Mask	Pass			Figure 10
12	Sensitivity		45	μW	@BER=10 <sup>-12</sup>

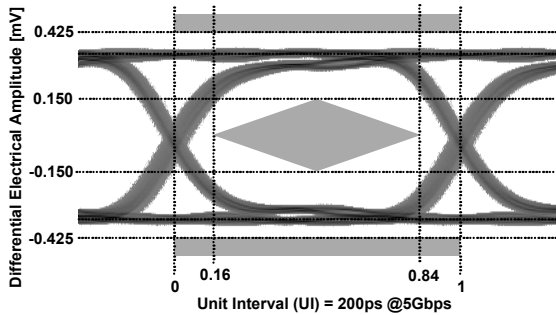


Figure 10: Rx eye diagram and Rx mask definition.

The absolute mask of Figure 10 defines the limits for the electrical swing and is based on the SFP+ high-speed specification (XFI) with the horizontal limits adjusted to the previous jitter specification and to our test set-up. This is a simple pass/fail test and we do not quantify the margins.

### C. TRx Power Dissipation

The TRx power dissipation is evaluated by measuring the current being supplied to the testboard when the TRx is operating in optical loopback. The testboard is required to be a clean board (no electronics) or we must be able to subtract the current supplied to the testboard electronics.

As point 13 of our specification, we propose a maximum of 600mW of TRx power dissipation (end-of-life value and across all operating temperatures). Our experience with commercial TRxs tells us that this specification might be too demanding for non VCSEL-based modules.

## IV. RESULTS

The previous test set-ups can generate a very large data set and we will focus on the TRx performance at 5Gbps. We flagged the devices that do not meet our specification proposal for 5Gbps operation and we developed a Figure of Merit (FoM) to combine all the performance data into three numbers:  $Tx_{FoM}$  for the Tx,  $Rx_{FoM}$  for the Rx and  $Pwr_{FoM}$  for the TRx power dissipation.

The FoM numbers are defined in the following three expressions, in which the weight factors were chosen to reflect our assessment of the relative performance of all twelve devices. The Tx mask margin has a value between 1 and 2 if the eye passes the mask test and a value lower than 1 if it does not. If the TRx performance equals the specification in every point then the FoM value is 100, but a value higher than 100 does not necessarily mean that the device complies with all points of the specification.

$$Tx_{FoM} = \frac{100}{15} \times \left( \frac{OMA}{OMA_{spec}} + \frac{Rise_{spec}}{Rise} + \frac{Fall_{spec}}{Fall} + 3 \times \frac{Tj_{spec}}{Tj} + \frac{Dj_{spec}}{Dj} + 3 \times \frac{Closure}{Closure_{spec}} + \frac{ER}{ER_{spec}} + FullMaskM + 3 \times CenterMaskM \right)$$

$$Rx_{FOM} = \frac{100}{10} \times \left( 6 \times \frac{Sensitivity_{Spec}}{Sensitivity} + 3 \times \frac{Tj_{Spec}}{Tj} + \frac{Dj_{Spec}}{Dj} \right)$$

$$Pwr_{FOM} = 100 \times \frac{Power_{Spec}}{Power}$$

The FoM results for our twelve devices under test are shown in Figure 11. The upper graph is the Tx performance, the middle is the Rx performance and the lower is the TRx power dissipation. The vertical scale is in arbitrary units and dashed gray bars indicate that at least one of the specification points has not been met.

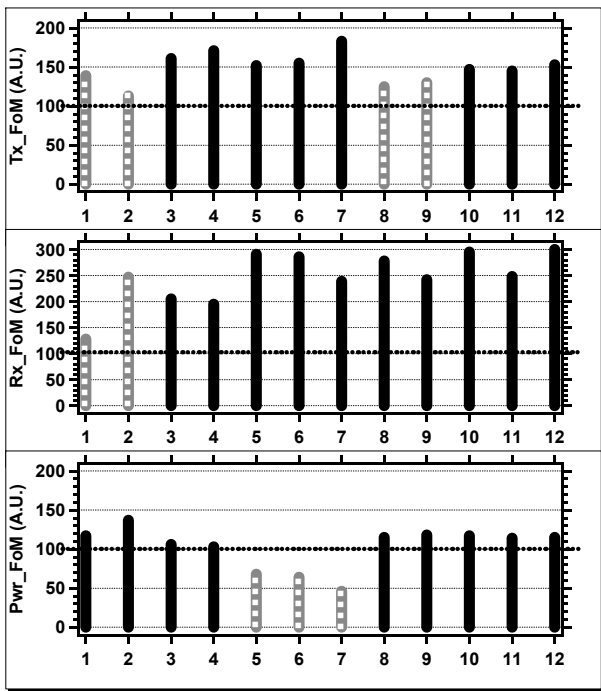


Figure 11: FoM results of all 12 TRxs under test (dashed gray=fail).

Devices 1 and 2 are SFP modules which are not fast enough to meet our specification for 5Gbps operation. Both modules have Tx problems with rise/fall times or jitter and both have Rx jitter problems. The power dissipation is below 600mW because the two modules are VCSEL-based (850nm and 1310nm).

The two 850nm VCSEL-based SFP+ (devices 3 and 4) have very good Tx performance and also a power dissipation below 600mW. The sensitivity of their PINs at 850nm is around -16dBm, i.e. about 2.5dB better than our specification.

The two 1310nm DFB-based SFP+ (devices 5 and 6) have good Tx performance at 5Gbps but their power dissipation is well above our specification (around 900mW). Due to the CDR circuitry of device 7 – a 1310nm DFB-based XFP – the Tx performance is very good but the power dissipation is even higher (around 1.3W). The Rx sensitivity of devices 5 and 6 is around -19dBm and the Rx sensitivity of the XFP module is about 2dB worse.

Devices 8 to 12 are 1310nm VCSEL-based SFP+ modules which makes possible power dissipations below 600mW. The 1310nm VCSELs are not yet a mature technology but the

performance of most modules is suitable for 5Gbps operation even if the Tx's have considerable overshoot and ringing.

The Rx sensitivity of all modules was found to be above the specification (45μW or -13.5dBm), but the two SFP modules are not able to meet the Rx jitter budget. The sensitivity of 1310nm modules was found to be a few dB better than the sensitivity of 850nm modules.

## V. CONCLUSIONS

The future VTRx modules will be built from radiation-qualified optoelectronic components by customizing a commercial TRx with ASICs sourced by the GBT project.

Using commercial devices we have developed test methods for TRx testing and a FoM that allows a quick and easy comparison of different modules. This enabled us to select a TRx type for VTRx customization and will allow us to evaluate the performance of the future prototype VTRx modules.

The results from our evaluation of twelve commercial TRxs show that the SFP+ is the most suitable candidate for VTRx customization and that we should target a VCSEL-based VTRx to achieve low power dissipation.

Our evaluation of TRxs also shows that, although 1310nm VCSELs are not yet a mature technology, there are diodes capable of being operated at 5Gbps with sufficient performance.

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