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Radiation qualification of the front-end electronics for the readout of the ATLAS liquid argon calorimeters

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ABSTRACT: The ATLAS detector has been built to study the reactions produced by the Large Hadron Collider (LHC). ATLAS includes a system of liquid argon calorimeters for energy measurements. The electronics for amplifying, shaping, sampling, pipelining, and digitizing the calorimeter signals is implemented on a set of front-end electronic boards. The front-end boards are installed in crates mounted between the calorimeters, where they will be subjected to significant levels of radiation during LHC operation. As a result, all components used on the front-end boards had to be subjected to an extensive set of radiation qualification tests. This paper describes radiation-tolerant designs, radiation testing, and radiation qualification of the front-end readout system for the ATLAS liquid argon calorimeters.

KEYWORDS: Radiation damage to electronic components; Front-end electronics for detector readout; Calorimeters.

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1. Introduction

The Large Hadron Collider (LHC) has been built at the CERN Laboratory in Geneva and will soon become operational for physics research [1]. The LHC is a high luminosity proton-proton collider operating at the centre of mass energy of 14 TeV. The high luminosity ($10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$) gives rise to an intense radiation environment that the detectors and their corresponding electronics must withstand.

The ATLAS detector is a multi-purpose apparatus constructed to exploit the new particle physics opportunities offered by the LHC [2]. The energy of the created particles will be measured by a novel calorimeter technique that employs liquid argon. The front-end electronics of the ATLAS liquid argon calorimeter is a mixed analog and digital processing system [3]. To record with high precision the large dynamic range signals from the liquid argon calorimeter and limit the coherent noise requires embedding a substantial portion of the electronic system inside the ATLAS detector volume. This inaccessible location sets stringent constraints on the design of the front-end electronics and its reliability. Thus the problems due to high radiation fields, limited access, and limited space had to be solved. A variety of technologies including GaAs, bipolar, BiCMOS, Silicon-on-Insulator (SOI), and commercial deep submicrometer (DSM) CMOS were employed in both radiation tolerant technologies and components off the shelf (COTS).

Figure 1 shows a block diagram of the electronic system for the liquid argon calorimeters of ATLAS. The entire system consists of approximately 190 000 channels. The motherboards are attached directly to the calorimeter electrodes and are immersed in liquid argon, which is contained in a cryostat. Access to this electronics should, ideally, never be necessary. The on-detector electronics is housed in 58 front-end crates that sit inside the ATLAS detector, but are mounted on the outside of the cryostat. Within the front-end electronic system are front-end boards, tower builder boards or tower driver boards, calibration boards, and controller boards. The off-detector electronics consists of digital storage and processing units, and a global ATLAS-wide trigger system. The data-handling portion of this electronics is housed in 60 readout crates. The off-detector electronics is readily accessible and is not in a radiation environment. Only the electronics on the motherboards in the cryostat and in the front-end crates receive significant levels of radiation.

2. ATLAS radiation environment

The radiation in the ATLAS detector is predominately secondary particles produced by interactions of the primary particles, from the interaction region, with the detector elements. As such, the energies are rather low (less than a few GeV), the fluxes are high, and the direction of the radiation fields on the electronics is homogenous. Figure 2 shows a radiation map of the total ionizing dose in the region of the calorimeter electronics. The electronic crates are located at a radial distance from the beam line (z-axis) of $R = (290 - 340)$ cm; the crates for the electromagnetic barrel calorimeter are located at a longitudinal position of $Z = \pm(300 - 350)$ cm and the end-cap calorimeter crates are located at $Z = \pm(620 - 670)$ cm. Figure 3 shows the corresponding radiation map for non-ionizing energy loss. The radiation map of hadrons and neutrons capable of causing single-event effects (SEE) in electronics is shown in figure 4. One can see in all three radiation maps that the radiation fields in the region of the crates for the electromagnetic barrel calorimeter is higher

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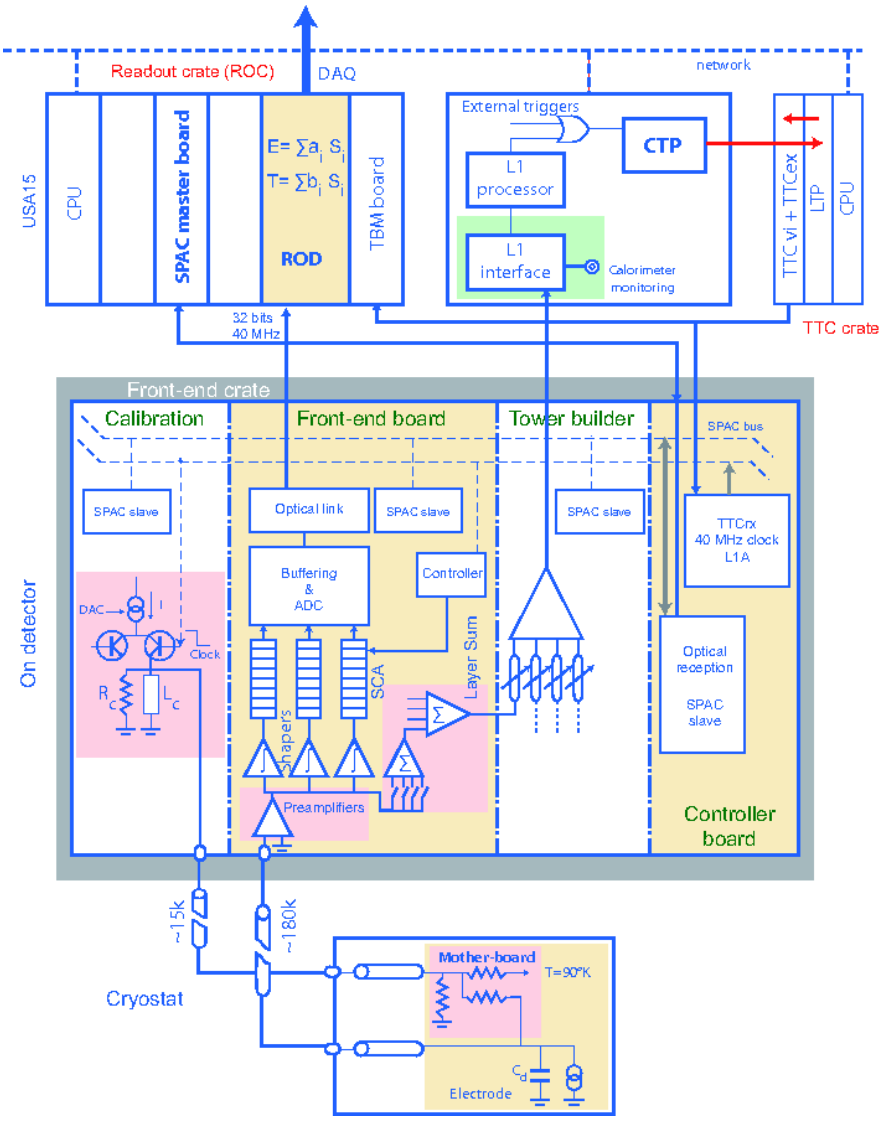

Figure 1. Block diagram of the electronic system for the ATLAS liquid argon calorimeter [3].

than for other regions at similar radial distance from the beam line. This is due to the particles "finding their way up" the crack between the barrel and end-cap calorimeters. The electronics for the end-cap calorimeters is mounted further from the interaction point, and thus the particle fluxes are less by about an order of magnitude than those at the location of the electromagnetic barrel calorimeter electronics.

Figure 5 shows the simulated energy spectra of gamma, neutron, electron, pion, and proton radiation in the region of the electromagnetic barrel liquid argon calorimeter electronics; these are the predominant radiations [4]. The fluxes of ions and other hadrons are less than the proton flux by about one order of magnitude, and the muon flux is less than the proton flux by about a factor of three.

The dominant type of radiation flux is photons and neutrons. Total ionizing radiation is mainly

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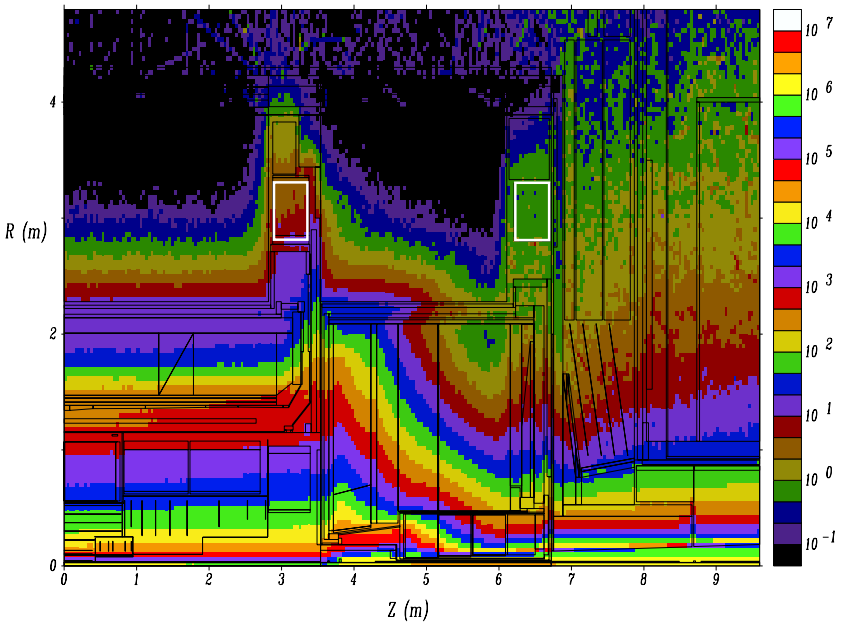

Figure 2. Total ionizing dose (Gy/yr) map for one year (10^7 s) of LHC operations at nominal luminosity $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The white boxes show the positions of the front-end crates in the barrel and end-caps.

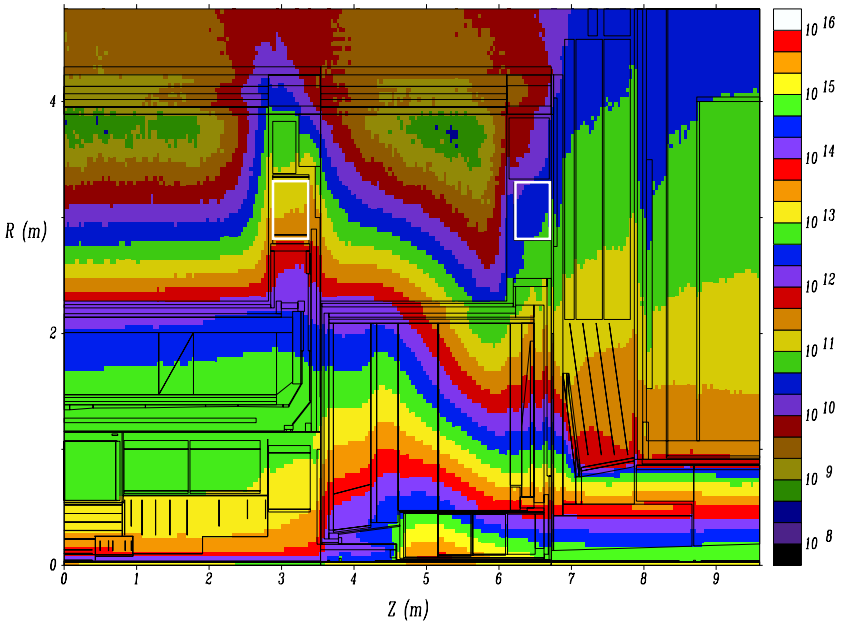

Figure 3. Non-ionizing energy loss (cm^{-2}/yr 1-MeV neutron equivalent in Si) map for one year (10^7 s) of LHC operations at nominal luminosity $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The white boxes show the positions of the front-end crates in the barrel and end-caps.

due to photons and neutrons at a level of about 5 Gy/yr.[1] Neutrons are the main contributors to the non-ionizing energy loss at a level of $2 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{yr}^{-1}$ (1-MeV neutron equivalent in Si).

[1]Throughout this paper, a year is considered to be a year of ATLAS operation, which is taken to be 10^7s at a luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

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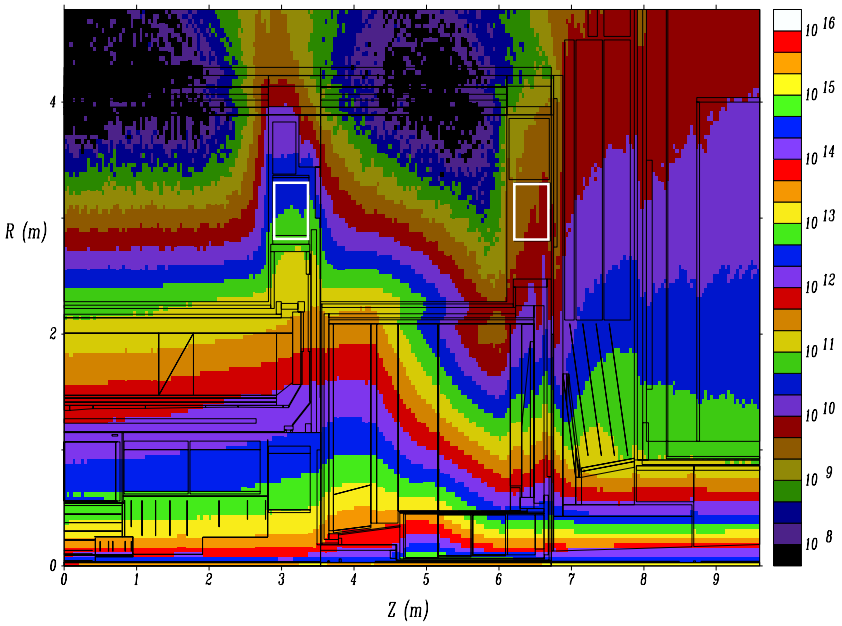

Figure 4. Hadron and neutron flux (cm^{-2}/yr energy greater than 20 MeV) map for one year (10^7 s) of LHC operations at nominal luminosity $10^{34}\,cm^{-2}s^{-1}$. The white boxes show the positions of the front-end crates in the barrel and end-caps.

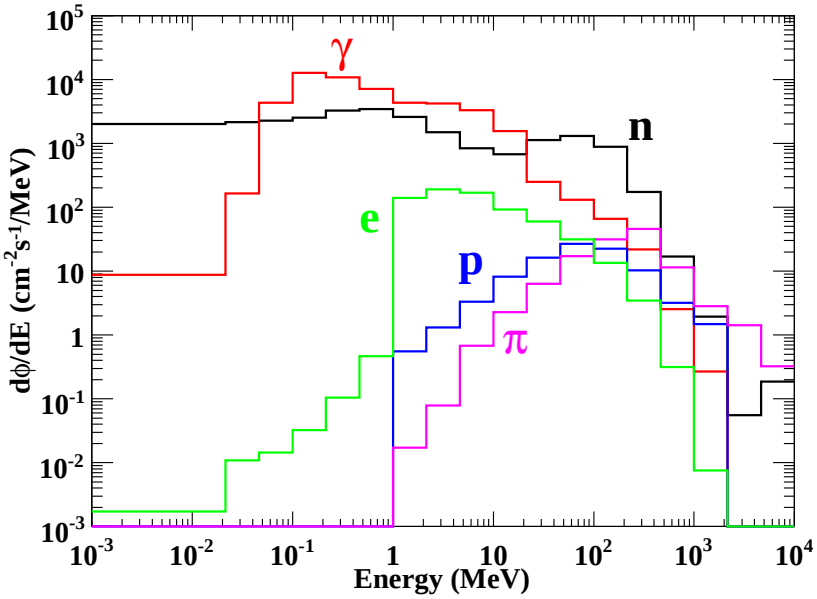

Figure 5. Particle flux versus energy in the region of the front-end electronics of the ATLAS electromagnetic barrel liquid argon calorimeter.

Also contributing to the radiation problem are charged hadrons (mainly protons and pions) and neutrons at a rate in excess of $4 \times 10^3\,cm^{-2}s^{-1}$ (with energy above 20 MeV), which could cause SEE in electronics.

It is planned to operate the electronics for a period of 10 years with limited access. Thus the

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Table 1. Some particle fluences after 10 years of LHC operation for various lower energy cutoffs in the region of the front-end electronics of the ATLAS electromagnetic barrel liquid argon calorimeter.

Radiation Type	Lowest Energy	Fluence (cm^{-2}/10 yr)
photons	100 keV	4.45×10^{12}
neutrons	100 keV	1.83×10^{12}
electrons	100 keV	6.99×10^{10}
neutrons	21 MeV	3.51×10^{11}
pions	21 MeV	1.16×10^{10}
protons	21 MeV	8.02×10^{9}

radiation tolerance levels used in this paper correspond to fluences after 10 years of radiation. Table 1 shows some simulated radiation fluences for 10 years of operation at the LHC in the region of the front-end electronics of the ATLAS electromagnetic barrel calorimeter. From figure 5 one can see that there is a substantial flux of photons and neutrons below the energy thresholds in table 1.

3. ATLAS policy on radiation-tolerant electronics

A high level of reliability of the electronics must be maintained during the 10 years of operation of the experiment. In most cases replacing components is not an option. To achieve a high reliability, a detector-wide radiation policy was developed that includes strategies for the pre-selection, qualification, and purchase of electronic components [5, 6].

Experience with space and military applications of radiation-tolerant electronics has shown it to be necessary to define specifications that the different components must meet. Within ATLAS, a choice can be made to use a radiation-tolerant process or otherwise do more testing to qualify particular COTS component. For radiation-tolerant application specific integrated circuits (ASICs), the results of standard radiation tests were compared to radiation-tolerance criteria in order to qualify the architecture and the design of the ASIC. For COTS, the results of standard radiation tests were compared to radiation-tolerance criteria in order to pre-select or to reject generic components, and to qualify or to reject lots of components.

The ATLAS policy on radiation tolerant electronics is a guideline. Deviations from the policy could be discussed with a reviewing body on a case-by-case bases. For example, the preamplifier, pre-shaper amplifier, and shaping amplifier were not tested for SEEs. This is because these parts contain analog circuits. It is unlikely that protons or neutrons would have large enough linear energy transfer (LET) to cause any single-event latch-up in these devices. While heavy ions may have large enough LET to cause latch-up, we do not anticipate large fluxes of heavy ions in the region of the calorimeter electronics.

3.1 Strategy for electronic component procurement

The strategies for the procurement of radiation-tolerant ASICs and COTS differ. For radiation-tolerant ASICs, a technology must be selected whose radiation tolerance complies with a set of radiation-tolerance criteria. Ideally, the radiation-tolerance level of the electrical parameters of the

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elementary components that are used for ASIC designs are guaranteed by the manufacturer. The ASICs may be developed using the selected radiation-tolerant technology, or using a radiation-soft technology plus a translation of advanced prototypes into the selected radiation-tolerant technology. Some technologies are not developed to be radiation tolerant, but the ASICs manufactured in these technologies can be made so if special layout techniques are employed. The ASICs may also be developed with layout techniques that are proven to be radiation tolerant. The robustness of the architecture and the design against radiation are the responsibility of the ASIC developer. The development phase should include radiation-tolerance tests made on advanced prototypes designed with the radiation-tolerant technology. The aim of these tests is to verify and, if necessary, improve the robustness of the architecture of the circuit against radiation. The final prototype designed with the radiation-tolerant technology must be qualified. This qualification process is based on the ATLAS standard test methods (see section 3.3). If the radiation tolerance of the final prototype satisfies the radiation tolerance criteria, lots of ASICs manufactured with the selected radiation-tolerant technology can be purchased.

The procurement process for COTS is more involved. First, the components of interest must satisfy the radiation-tolerance criteria. This identifies part numbers and manufacturers of generic components that can be considered for use in ATLAS, however, it does not select the actual physical parts that can be used in ATLAS. Lots of these components must be radiation qualified to be used in ATLAS. Ideally, the purchase of qualified lots of components occurs after the qualification step. This requires a good relationship with the vendor, who must agree to "freeze" homogeneous lots and to provide samples that the customer will test before deciding to purchase or reject the frozen lots. Most of the time, vendors cannot freeze lots and the lots must be purchased first. This induces a risk of purchasing bad lots.

3.2 Radiation-tolerance criteria

To quantify the qualification process, a set of radiation-tolerance criteria has been developed. The criteria result from simulated radiation levels multiplied by safety factors. Simulated radiation levels were computed for each region of the ATLAS detector. Some examples of the simulated radiation levels in the region of the electronics for the electromagnetic barrel liquid argon calorimeter were shown in figure 5 and table 1.

The results of the simulated radiation levels are calculated in cells of $\Delta R \times \Delta Z$ of size $10\,\text{cm} \times 10\,\text{cm}$, spanning all azimuthal angles; azimuthal and mirror symmetry about the beam-crossing point are assumed. The cell with the highest radiation level within the larger crate region is taken to represent the radiation level received by the electronics. Total ionizing dose (TID) is calculated as the simulated ionizing energy absorbed in each cell divided by the mass of material in that cell. Thus any particle which deposits energy in the form of ionization can contribute to TID. The non-ionizing energy loss (NIEL) is calculated by simulating the particle fluences and convolving the energy spectra with silicon displacement-damage functions, normalized to the value of the damage function for 1-MeV neutrons in silicon (Si) [7]. Thus NIEL is expressed as the equivalent effect in Si of a 1-MeV kinetic energy neutron flux in cm^{-2}/yr. The SEE rate is calculated by summing the rates of charge hadrons and neutrons with kinetic energies greater than 20 MeV. In this way, the simulated radiation levels for the electronics of the barrel electromagnetic liquid

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Table 2. Radiation-tolerance criteria of ASICs in a radiation tolerant process for total ionizing dose (TID), non-ionizing energy loss (NIEL) (1-MeV neutron equivalent in Si), and single-event effects (SEE) (> 20 MeV hadrons) in the region of the front-end electronics of the ATLAS electromagnetic barrel liquid argon calorimeter.

Test	Pre-Selection	Qualification
TID	1.2×10^3 Gy	5.8×10^2 Gy
NIEL	3.3×10^{13} cm^{-2}	1.7×10^{13} cm^{-2}
SEE	6.3×10^{12} cm^{-2}	3.2×10^{12} cm^{-2}

argon calorimeter are TID 10 Gy/yr, NIEL 3×10^{11} cm^{-2}yr^{-1} (1-MeV neutron equivalent in Si), and SEE 6×10^3 cm^{-2}s^{-1}.

Safety factors were used to account for the simulation uncertainties of the radiation levels, uncertainties in low-dose rate effects in TID testing, and variations of radiation tolerance from lot to lot and within lots of components. The simulation safety factors accounting for uncertainties in the event generation models, the transport models, the physical description of the detector, and limited statistics are 3.5 for TID, 5 for NIEL, and 5 for SEE.

The low-dose rate effect is an increase in the damage produced by TID on CMOS, JFET, or bipolar devices when exposed to radiation at low rates [8 – 11]. The safety factors to account for this are 5 for COTS and 1.5 for radiation-tolerant ASICs.

Radiation tolerance of components can vary from batch to batch. We define a homogeneous batch as a batch of components issued from wafers manufactured together at the same time on a known production line. We define an unknown batch as a batch of components provided by a vender without information on the production line, on the batch number, etc.; these components may be issued from different batches or different production lines. A safety factor of 2 is applied to pre-selecting COTS or radiation-tolerant ASICs issued from homogeneous batches, or from unknown batches if their qualification is to be done on homogeneous batches. A safety factor of 4 is applied for the pre-selection of COTS issued from unknown batches if their qualification is to be done on unknown batches, or for the qualification of unknown COTS batches.

The radiation-tolerance criteria for radiation-tolerant ASICs and COTS for total ionizing dose, non-ionizing energy loss, and single-event effects are shown in table 2 and table 3. These are the criteria that must be satisfied for electronic component procurement in the region of the ATLAS electromagnetic barrel liquid argon calorimeter. Typical, radiation-tolerance criteria are lower for the qualification than the pre-selection because there is some reduction in uncertainty at the qualification stage if the components have already passed the pre-selection criteria.

3.3 Standard test methods

ATLAS standard test methods are derived from DOD or ESA test methods [12 – 14] for CMOS devices and from ref. [15] for bipolar or BiCMOS devices, with several modifications that take into account the unique radiation environment in ATLAS. All test results must be documented in standard report forms which are then approved by the ATLAS Radiation Hardness Assurance Working Group.

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Table 3. Radiation-tolerance criteria of COTS for total ionizing dose (TID), non-ionizing energy loss (NIEL) (1-MeV neutron equivalent in Si), and single-event effects (SEE) (> 20 MeV hadrons) in the region of the front-end electronics of the ATLAS electromagnetic barrel liquid argon calorimeter.

Test	Pre-Selection		Qualification	
	unknown qualification batches	known qualification batches	unknown batches	known batches
TID	7.8×10^3 Gy	3.9×10^3 Gy	7.8×10^3 Gy	1.9×10^3 Gy
NIEL	6.6×10^{13} cm^{-2}	3.3×10^{13} cm^{-2}	6.6×10^{13} cm^{-2}	1.7×10^{13} cm^{-2}
SEE	1.3×10^{13} cm^{-2}	6.3×10^{12} cm^{-2}	1.3×10^{13} cm^{-2}	3.2×10^{12} cm^{-2}

The ATLAS standard TID test method enabled us to measure the effects of total ionizing dose, for example, the cumulative energy deposited in the oxides of CMOS electronic components. TID test methods were based on gamma-ray or X-ray exposures.

A brief summary of the test method for pre-selecting generic CMOS components from a known batch that satisfy the TID radiation tolerance criteria is as follows. Eleven functioning parts are selected for the test. Electrical measurements are preformed on the parts. One part is selected at random to be the non-exposed reference part. All 10 parts are exposed to a gamma source until the TID radiation-tolerance criterion is reached or exceeded. The TID can be applied in one or several steps. Electrical measurements are performed on each part within one hour after the end of each exposure step. The next step must be within three hours of the previous step. At the end of the final exposure, the parts are annealed for 24 hours at 20°C, after which the electrical measurements are repeated. If the electrical parameters have not changed significantly after annealing, the generic component can be accepted for ATLAS, else it is rejected. The same procedure is applied to the qualification of a batch of components, and for the pre-selection and qualification of bipolar and BiCMOS devices.

The ATLAS standard NIEL test method enabled us to measure the effects of particles exhibiting non-ionizing energy loss. These particles produce displacement damage in silicon, which degrades the electrical parameters of electronic components. The NIEL test method was based on neutron exposures. NIEL testing of pure CMOS devices was not required since they are naturally tolerant to displacement damage [5].

A brief summary of the test method for pre-selecting generic components and for qualifying batches of components from a known batch that satisfy the NIEL radiation tolerance criteria follows. For the pre-selection of generic components, 11 functioning parts must be used. Electrical measurements of the main AC and DC parameters relevant to the device are performed on all the parts. One part is selected at random to be the non-exposed reference part. The 10 parts are exposed to neutron radiation up to or exceeding the radiation-tolerance criteria. The neutron fluence can be applied either in one single step or in several steps. In the case of several steps, the electrical measurements should be performed online during exposure. After the exposure, the electrical measurements are repeated on all 11 parts. If the electrical parameters of all 10 exposed parts are similar to the values before exposure, the device is accepted as a generic component, else it is rejected. The same procedure applies to the qualification of batches of components to determine the acceptance or rejection of the batch of components.

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The ATLAS standard SEE test method enabled us to estimate SEE rates (upset, latch-up, burnout, gate rupture, etc.) expected in a given ATLAS environment. This test method was primarily based on proton exposures, but could also be performed using neutrons (with high enough energy). Protons with an energy between 60 MeV and 200 MeV can be used to measure soft SEE rates. Soft SEEs are radiation induced bit flips that corrupt data or system configurations. They are not permanent effects — they can be cancelled by resetting the system or rewriting data in a memory. However, an exhaustive search for soft, hard, and destructive SEE requires protons with energy between 200 MeV and 500 MeV. Hard SEEs are radiation induced bit flips that corrupt data and system configurations. They are permanent effects — they can not be cancelled by resetting the system or rewriting data in memory. Destructive SEE produce permanent short circuits (e.g., latch-up, burnout, gate rupture). Latch-up can be nondestructive if mitigating or protective circuits are employed in the circuit architecture. The SEE test method applies only to the pre-selection of generic components. It was not required for the qualification of lots since the results of pre-selection tests should be reproducible and thus applicable for qualification.

A brief summary of the test method for the pre-selection of integrated circuits satisfying the SEE radiation-tolerance criteria using proton beams is as follows. The method for using neutrons or more detail of the method for protons can be found in ref. [5]. Five working parts are selected. Electrical measurements are performed on the five parts. One part is selected at random as the reference and is not exposed to radiation. The four remaining parts are exposed to a proton beam of a constant flux. The total fluence must be large enough to produce a total number of SEU large enough for estimating upset rates in ATLAS with adequate statistics. The power consumption during exposure must be automatically and continously measured. Digital circuits must be automatically and periodically written to and read from to search for temporary or permanent bit errors; analog circuits must be automatically and continously read to search for parasitic transient pulses. Online measurement and recording of soft, hard, and destructive SEE must be made during the entire radiation exposure. If any part fails due to a destructive SEE these devices can not be used in ATLAS. Based on the proton fluence and number of observed non-destructive SEU, the failure rate of the device in the ATLAS radiation environment is estimated. If this rate is below acceptable limits, the generic components are acceptable for ATLAS, else they are rejected. No additional qualification is required.

Photons are recommended for TID testing, neutrons for NIEL testing, and protons for SEE testing. However, it was often more efficient to simulate all these types of damage using a single radiation source. Protons with energy of about 160 MeV — a typical energy that we used — deposit more energy in silicon than minimum ionizing particles and thus give TID. Protons of these energies also cause about 0.74 times as much damage as 1-MeV neutron equivalent in silicon [16]. The conversion factors in both cases are energy dependent [7]. Thus proton exposures were sometimes used to simulate the effects of TID and NIEL, as well as cause SEEs. In addition, neutron sources, particularly reactors, are contaminated with photons and thus neutron exposures, if properly calibrated, can also satisfy TID testing. We characterized several radiation facilities and pooled our testing resources. Table 4 lists some of the radiation facilities used to radiation qualify the front-end electronics.

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Table 4. Some of the facilities used to radiation qualify the front-end electronics for the readout of the ATLAS liquid argon calorimeters. The third column lists the names of some of the ATLAS liquid argon calorimeter components tested at the facilities, as will be described in more detail later.

Photon Radiation Facilities		
Cosase Saclay (^{60}Co)	Gif-sur-Yvette, France	HAMAC
Pagure Saclay (^{60}60)	Gif-sur-Yvette, France	shaper, AD8001, AD8011, HFA1135, BIMUX
U. of Alberta (X-rays)	Edmonton, Canada	SCAC
Brookhaven National Laboratory (BNL) (^{60}Co)	Upton, USA	warm preamps, HFA1135, HDMP-1022, OTx, fiber
Neutron Radiation Facilities		
IBR-2 reactor	Dubna, Russia	GaAs preamp, pre-shaper
IRRAD-2 PS CERN	Geneva, Switzerland	SCAC
CERI (cyclotron)	Orleans, France	shaper, HAMAC, HFA1135
ULYSEE Saclay	Gif-sur-Yvette, France	BIMUX, AD8001, AD8011, HFA1135
SARA (cyclotron)	Grenoble, France	warm preamps
Lowell Radiation Lab.	Lowell, USA	HFA1135
Proton Radiation Facilities		
OPTIS PSI	Villigen, Switzerland	SPAC slave, AD9042
Louvain la Neuve	Louvain-la-Neuve, Belgium	BIMUX, CALOGIC
PIF TRIUMF	Vancouver, Canada	SCAC
HCL Harvard	Cambridge, USA	CONFIG, SCAC, AD8042, MC10H116
NPCT MGH	Cambridge, USA	SCAC, GSEL, CLKFO, QPLL, LHC7913, AD8042, MC10H116

4. Some methods used to improve radiation tolerance

The components in the front-end electronic system are implemented using several different technologies. Sixteen radiation-tolerant ASICs were produced for the front-end electronics (see table 5). Each major component needed to pass a production readiness review before it could be manufactured or purchased in production quantities.

Some components were first prototyped in semiconductor processes known to be radiation soft to prove the design. The designs were then migrated, along with any corrections, to radiation tolerant technologies. Much of the digital electronics was prototyped in field programmable gate arrays (FPGA). Because of the attractiveness of using FPGAs, prototypes were also radiation tested to understand the circuit failure mechanisms, and if the designs could be made radiation tolerant and be potentially viable. All the programmable devices we tested caused the power-supply current to increase before a TID of 830 Gy(SiO_2), and well below the TID radiation-tolerance criteria for pre-selecting COTS [17, 18]. By measuring the proton upset cross section and convoluting with the ATLAS proton energy spectrum, we predicted one bad channel for a period of a few seconds occurring about every minute on average if FPGAs were used to control the switched capacitor arrays on the front-end boards [19]. These effects were consider unmanageable and the circuit designs were migrated to ASICs.

The first radiation-tolerant technology we used was DMILL. DMILL was a BiCMOS radiation

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Table 5. The acronyms of the main active components in the front-end electronic system and the component's functionality. The components are grouped according to the semiconductor technology used in their production.

Production Process	Component	Functionality
Hybrid	warm preamp	first-stage amplification (outside liquid Ar)
	pre-shaper	amplification, pre-shaping for hadronic end-cap calorimeter
TriQuint GaAs	cold preamp	first-stage amplification (in liquid Ar)
AMS BiCMOS	shaper	amplification and shaping
DMILL	op-amp	low-offset amplifier for calibration
	HAMAC	switched capacitor array (SCA)
	SPAC slave	serial control interface
	CONFIG	configuration controller
	SMUX	32:16 multiplexer
	BIMUX	dual 8:1 passive analog multiplexer
	DAC	calibration board DAC
	CALOGIC	calibration control
	PHOS4	0-24 ns, 1ns step delay
	TTCrx	trigger and timing control receiver
DSM	GSEL	gain selection, data formatting
	SCAC	SCA controller
	CLKFO	clock fanout
	QPLL	quartz-crystal phase-locked loop
	DCU	temperature and voltage monitor
STm RHBip1	LHC4913	positive-voltage regulator
	LHC7913	negative-voltage regulator
COTS	HFA1135	360 MHz, video op-amp with output limiting
	MC10H116	ECL triple-line receiver
	AD9042	12-bit, 41 MSPS monolithic A/D converter
	AD8042	dual 160 MHz rail-to-rail amplifier
	AD8011	300 MHz, 1 mA current feedback amplifier
	AD8001	800 MHz, 50 mW current feedback amplifier
	HDMP-1022	Gigabit rate serializer with TTL I/Os
	SY88922V	2.5 Gbps laser diode driver
	TTR-1A43	850 nm high power VCSEL
	TRR-1B43	155 Mbps InGaAs PINTIA

hard technology which was offered by TEMIC Matra MHS [20]. It was a mixed analog and digital process radiation hardened to tolerate a combination of 100 kGy and neutron fluence of 10^{14} cm^{-2}. The process was manufactured with SOI and had two metal layers. A trench technique was used to isolate the active areas in order to remove the latch-up inherent to CMOS technology. The minimum lithography was 0.8 μm, which allowed about one million transistors per square centimeter. The technology was 5 V and was good for analog designs, but unfortunately is no longer available.

The radiation hardness assurance of the DMILL technology was achieved by monitoring the evolution of each sensitive parameter through exposures up to 100 kGy. Control of the tolerance of the technology was based on "statistical process control". In addition, regular extended radiation

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tests, including neutron and post-irradiation effects, were performed on specific mixed analog and digital test structures to verify the functionality and noise performance.

For many of the digital ASICs, a commercial DSM 0.25 μm CMOS technology with a radiation-tolerant layout technique was used [21, 22]. The layouts made systematic use of an enclosed transistor topology and guard rings to prevent any radiation-induced leakage current under the thick isolation oxide. The data-latch and SRAM standard cells have been designed to be single-event upset (SEU) resistant [23]. In the circuit designs, considerable mitigation techniques were employed to reduce the sensitivity to SEE. Error detection and correction (EDAC) logic, such as Hamming codes in the SRAM and triple-redundant registers with majority-voting logic, were used. In addition, careful attention was paid to design and simulation of the state machines to avoid lockup. System-level mitigation techniques on the front-end board and in the readout system have also been used.

5. Front-end electronics

This section describes the radiation qualification of the various components used on the electronic boards residing in the front-end crates. The section is organized according to which board the components sit on.

5.1 Front-end board

The front-end boards contain the electronics for amplifying, shaping, sampling, pipelining, and digitizing the liquid argon calorimeter signals [24]. Because of the large number of different ASICs on the front-end board and their unique solutions to radiation tolerance, we describe each of them separately.

5.1.1 Preamplifier

Preamplifiers must amplify the detector signals so that the resulting outputs are above the noise level of the downstream-stage electronics. The preamplifiers should thus be the dominant contributor to the electronic noise. They have to accept the entire signal dynamic range of greater than 16-bit and have high speed, which requires them to have low input impedance. Current preamplifiers are used which provide a voltage output directly proportional to the input current.

Most of the calorimeter is read out using warm preamplifiers which are mounted on the front-end boards [25]. These amplifiers are coupled to the detector through transmission lines of several meters in length. High-speed silicon bipolar transistors are used in these preamplifiers, and as a result, they should be adequately resistant to radiation damage. The preamplifiers were exposed to both gamma and neutron radiation. Preamplifiers from the pre-production were exposed under power to ^{60}Co gamma rays. A few exposed samples were 50 Ω impedance devices (part number IO823), while the others were 25 Ω impedance devices (part number IO824). Both hybrid types were measured for gain, peaking time, equivalent noise current (ENI), and input impedance before exposure and after total doses of 500 Gy and 1 kGy. The gain, peaking time, and ENI changed by less than the measurement error for both hybrid types after 500 Gy. Table 6 shows that the input impedance decreased at most 5% after an absorbed dose of 1 kGy [26].

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Table 6. Input impedance in ohms for the two preamplifier devices before and after exposure to ^{60}Co gamma rays.

	Un-exposed	500 Gy	1 kGy
IO823	51.3	50.1 (2.3% change)	48.8 (4.9% change)
IO824	25.4	25.3 (0.4% change)	25.2 (0.8% change)

The preamplifiers were also exposed to fast neutrons at SARA [27, 28] up to a neutron fluence of about 1×10^{14} cm^{-2} (1-MeV neutron equivalent in Si). No noise degradation was observed until a fluence of 5×10^{13} cm^{-2} was reached. The neutrons induced a degradation of the forward-gain β of the fast bipolar transistors used in the circuits. The β degradation followed the Messenger-Spratt relation [29] and, to first order, was inversely proportional to the cutoff frequency f_T. The impact of the β degradation of the transistors on the preamplifier resulted in about a 7% loss in gain after a neutron fluence of 1.1×10^{14} cm^{-2} for the 50 Ω preamplifiers, while the 25 Ω preamplifiers showed about a 3% gain loss after the same fluence. The measurement of the input impedance of all the exposed preamplifiers indicated that there was no stability problem due to radiation; all of them had a positive real part of the input impedance in a frequency range 1–200 MHz [30].

5.1.2 Pre-shaper amplifier

The hadronic end-cap calorimeter has its preamplifiers mounted directly on the calorimeter in the liquid argon. The preamplifiers output are driven on cables out of the cryostat to the front-end boards. Instead of the plug-in preamplifier hybrids used for the rest of the liquid argon calorimeter subsystem, the hadronic end-cap calorimeter front-end boards are equipped with plug-in pre-shapers. The role of the pre-shapers is to provide pole-zero cancellation to adapt to the widely varying hadronic end-cap detector capacitance, and invert, amplify, and pre-shape the signal so that the input to the shaper is the same polarity and approximately the same shape as the rest of the liquid argon calorimeters. This allows the same front-end board to be used for all liquid argon calorimeter subsystems.

Since the pre-shapers will be placed inside the end-cap front-end crates, it is necessary to radiation qualify them. A neutron exposure of 10 hybrids (40 channels) has been carried out at the IBR-2 reactor. The total neutron fluence was 2.7×10^{14} cm^{-2} and the corresponding total ionizing dose was 1.2 kGy. The accuracy of these dose measurements was about 10%. No significant changes due to TID were observed in the noise, linearity, or shaping time.

Figure 6 shows the signal amplitude versus neutron fluence for four different shaper time constants. The amplitude dropped by less than 3% after the NIEL radiation tolerance criterion of 9.6×10^{12} cm^{-2}. However, the drop was less than 1% for the shaping time of 25 ns, which is closest to nominal setting. The peaking time changed by less than 2% for 40 channels up to the total exposure. The response remained linear over the required 4 V dynamic range. After exposure, the noise was measured on the shaper output and then recalculated to the pre-shaper input. No change greater than the approximate 20% measurement error of the noise was observed. None of the 40 exposed channels died and no significant shifts in the parameters were observed. More details can be found in ref. [31].

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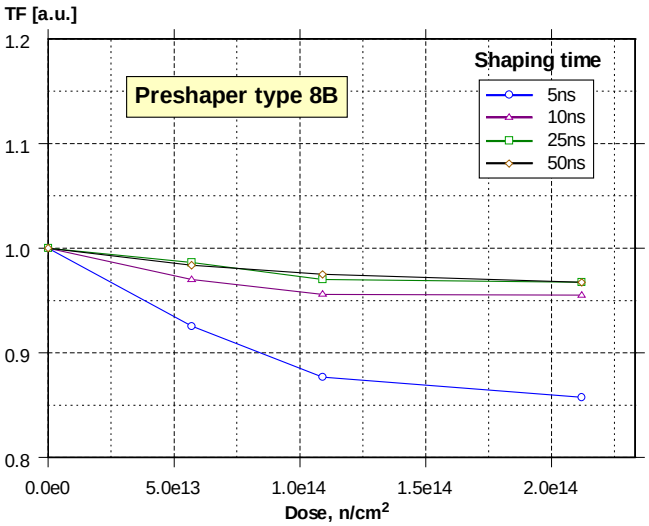

Figure 6. Amplitude during exposure relative to the amplitude before exposure versus neutron fluence for four shaping times of the hadronic end-cap calorimeter pre-shaper.

5.1.3 Shaping amplifier

Shaping amplifiers are used at the input to the sampling stage of the electronics. Their function is to limit the system bandwidth to match the 40 MHz sampling frequency. They are also required to minimize baseline shifts. A bipolar CR-$(RC)^2$ shaping function was used.

It is not possible to achieve a linear system using only a single gain scale without degrading the greater than 16-bit dynamic range of the input signal. Three gain ranges, each with a linear response, were used to extend the dynamic range. Thus for each input, the shaper produces three output signals.

The shaping amplifiers were built as integrated circuits using the Austria Mikro Systems (AMS) 1.2 μm BiCMOS technology, which should provide adequate immunity to radiation. Also, care in the design was used to provide additional radiation tolerance [32]. In the signal path, the shaper uses only fast NPN transistors operating at a relatively large current. MOS transistors are also used but in a configuration insensitive to their threshold voltage.

A prototype version of the chip showed satisfactory radiation tolerance to gamma rays and neutrons. For qualification testing, neutrons at CERI (same facility as SARA but moved to Orleans when SARA stopped operating) and gammas from the ^{60}Co source at Pagure were used. Figure 7 shows the amplitude versus TID and the peaking time versus neutron fluence. The change in gain or peaking time were insignificant and the chips showed satisfactory radiation tolerance.

The shaper incorporates a small section of simple digital logic to deactivate noisy channels in the trigger sums. SEUs in this logic would not be detrimental to the operation of ATLAS since the logic can be reloaded from time to time. Although latch-up was never observed in the 10 MeV neutron tests at CERI or 20 MeV proton fluences to 3×10^{13} cm^{-2}, an anti-latching resister was added in the logic power supply line for safety,

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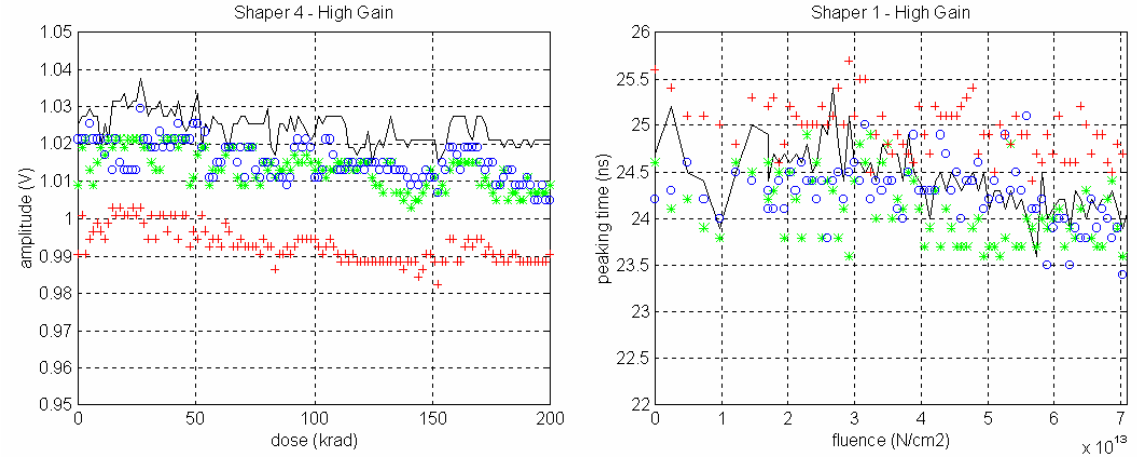

Figure 7. Shaper amplitude versus total ionizing dose and peaking time versus neutron fluence for four channels.

5.1.4 Switched Capacitor Array

Signals from the shaper outputs are sampled at 40 MHz and the results stored in an analog memory chip — switched capacitor array (SCA) — during the latency of the level-1 trigger (2.5 μs maximum). The analog pipeline is 144 cells deep.

Sixteen analog pipelines are integrated into an ASIC. Each ASIC thus services four calorimeter channels, each with three gains and a reference. To improve noise immunity, the reference is subtracted from the signal, for each channel, forming a quasi-differential structure. The ASIC is mostly analog with a few digital circuits. It contains about 45 000 transistors and 2 384 capacitors.

About 2 000 analog memory ASICs using a Hewlett-Packard process were produced for testing prototype calorimeters. The performance was very good. A radiation-tolerant version of the analog memory (HAMAC) was then migrated to the DMILL technology [33]. Since the HAMAC chip was manufactured in the DMILL technology no formal radiation testing was required. However, radiation tests were performed since the analog performance of the SCA is critical. The HAMAC circuits were operating during the tests. Operating the SCA in a radiation environment requires a quite complicated test setup, so fewer samples were tested.

Three samples, from two different batches, of HAMAC chips were exposed up to 3 kGy(SiO_2). The exposures were performed at Cocase. A dose rate of 1.4 Gy/hr was used. At the end of the exposures, the chips were still fully functional. The chips were tested within a day after the exposures. The change in power-supply current was smaller than the 1 mA accuracy of the test setup. The pedestal shifts were small with a mean value of zero over all channels (see figure 8). The change in noise and fixed pattern noise with dose were negligible. The voltage-droop rate of the pipeline storage cells might have changed after exposures because of possible current leakage appearing on NMOS switches. However, after exposure the voltage-droop rate remained smaller than 250 μV/460 μs.

Neutron exposures with fluence up to 3×10^{13} cm^{-2} ($\pm$20%) were performed at CERI. Taking into account the CERI energy spectrum, this fluence was equivalent to a 4.5×10^{13} cm^{-2} exposure with 1-MeV neutron equivalent in Si. Four chips, from three different batches, were exposed. The

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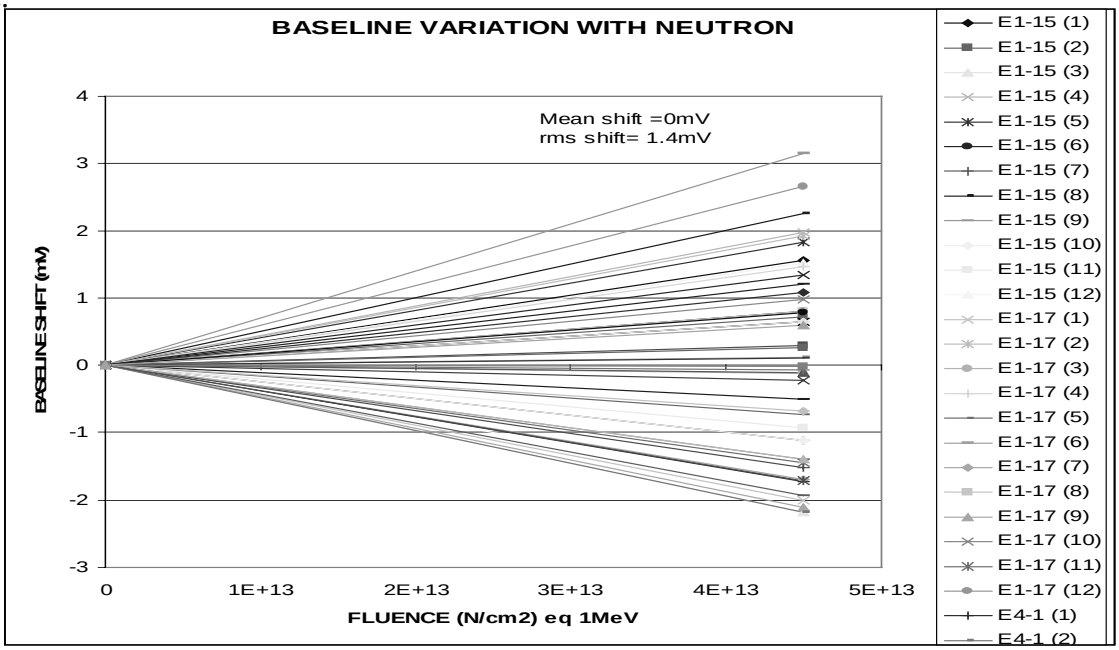

Figure 8. Baseline shift in mV (ordinate) versus neutron fluence for 48 channels of switched capacitor arrays.

chips were tested two months after the exposure, a period necessary to reduce their radioactivity. The change in power-supply current, pedestal, noise, and fixed pattern noise remained negligible after neutron exposure. The voltage-droop rate remained smaller than 250 μV/460 μs.

5.1.5 Analog to Digital Converter

Upon receipt of a trigger accept signal (75 kHz average rate) typically five samples around the peak of the pulse, originating at the triggered accelerator beam-crossing, are read from the switch capacitor arrays and multiplexed to a 12-bit commercial analog to digital converter (ADC) for digitization. One ADC digitizes the signals from eight calorimeter channels.

Two commercial AD8042 dual operational amplifier chips couple the SCA outputs to the ADC. The first pair of operational amplifiers are connected as emitter followers to provide high-impedance loads to the two pseudo-differential CMOS SCA output drivers. The second pair of operational amplifiers perform the differential subtraction in front of the single-ended ADC. In addition, they are operated with less than unity gain to map the SCA output voltage range onto the more limited ADC input signal range. Finally, they add in a voltage offset such that the SCA pedestal value corresponds to approximately 1 000 ADC counts, allowing measurements on both the positive and negative lobes of the shaped calorimeter signals.

The AD8042 was pre-selected by exposing the device to a proton beam of energy 148 MeV at the HCL. Four samples received at least a proton fluence of 1.1×10^{12} cm^{-2}, while a fifth sample received 8.5×10^{12} cm^{-2}; the corresponding TID was 78 krad(Si) and 310 krad(Si). During these tests, the non-inverting input was tied to ground and the inverting input was tied to the output via an *RC*-filter network. The voltages and currents were monitored during the exposure. The power-

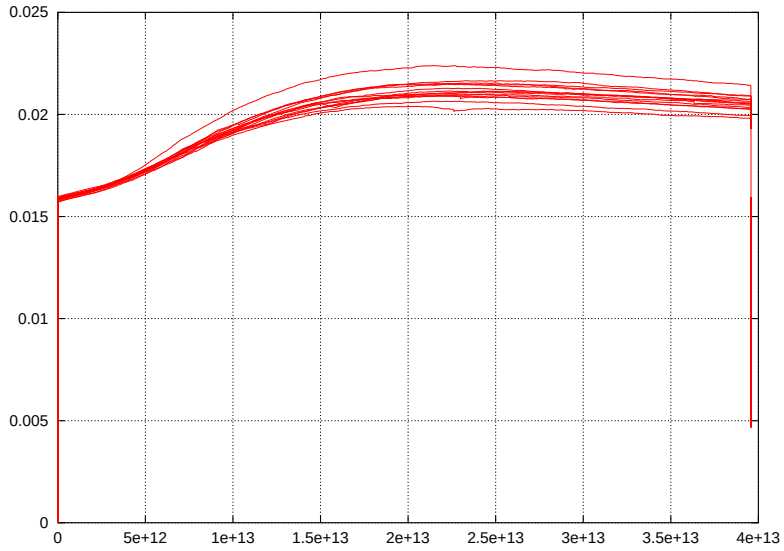

Figure 9. Current drawn by AD8042 dual operational amplifier chips as a function of proton fluence of energy 158 MeV.

supply current increased by about 1% per 10^{12} cm^{-2} proton fluence, or 80 krad(Si) of TID. No occurrence of latch-up was observed.

For the radiation qualification tests, a proton beam of energy 158 MeV at the NPCT MGH has been used. A results of the change in power supply current are shown in figure 9. This small change is acceptable.

The ADC used on the front-end board is the AD9042 from Analog Devices Inc. This device is a monolithic 12-bit 41 Msps ADC. The pre-selection of this chip was based on the test results from Ref [34]. In the study, ADC chips were exposed up to 2×10^4 Gy(Si) and to a neutron fluence of 4×10^{13} cm^{-2} (1-MeV neutron equivalent in Si). The signal to noise ratio (SNR) and the worst spur (WS)[2] were measured before and after the exposures. Chips from different wafers were also compared. Within the accuracy of the measurement, the results from the study qualified the AD9042 to be used on the front-end board.

The purchase of the ADC chips was conducted through CERN under a special purchase contract with Analog Devices Inc.. The ADCs were produced in four production lots. A production qualification test was added in the procurement contract. In each lot, 50 chips were randomly selected as qualification samples. These samples were grouped into two sets of 25 chips each. Radiation was applied to 24 chips in group one, while the 25th chip in that group was used as a reference and not exposed to radiation. The exposures were performed in two steps. In the first step, gammas from a ^{60}Co source were used and a total dose of 10 kGy(Si) was accumulated. In the second step, neutrons from a Californium source with a fluence of 2×10^{13} cm^{-2} (1-MeV neutron equivalent in Si) were used. The ADCs were under proper bias voltage during exposure. Key parameters such as the SNR, WS, and the reference voltage were measured before and after the exposures on all 25 chips. If any of the 24 exposed chips failed the criteria set in the contract, the

[2]Worst spur is defined as the power ratio of the highest non-fundamental frequency (usually the second harmonic) to the fundamental frequency.

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Table 7. Comparison of the measured parameters of the AD9042 before exposure to radiation with the data sheet values. The parameters are the signal to noise ratio (SNR), the worst spur (WS), and the reference voltage (Vref).

Parameter		SNR (dB)	WS (dBc)	Vref (mV)
Measured	Minimum	64.7	−88	2462
	Maximum	68.8	−66	2539
	Mean	67.6	−78	2484
	Standard deviation	0.5	3	14
	Measurement error	0.1	0.4	
Data Sheets	Minimum (25°C)	64		
	Typical (25°C)	67.0 – 68.0	−80	2400
	Maximum (25°C)		−73	
	Full temperature range	66.5 – 67.5	−78	

test would be repeated with the second group of 25 qualification samples. The lot would be rejected if the second group also failed.

An evaluation system was designed and constructed for the qualification tests. To characterize an ADC, one uses it to digitize a pure sine wave. The digital data are transformed into the frequency domain and analyzed. The dynamic performance of the ADCs is calculated based on the harmonics and noise when compared with the corresponding component in the input waveform [35].

We choose to measure the AD9042 at four frequencies (1.25 MHz, 2.50 MHz, 5.0 MHz, and 9.6 MHz) and at two input amplitudes (20 mV and 450 mV). The sine wave was sampled at 40.00 MHz and 8 192 consecutive digital sampling points were recorded. A total of 64 measurements were performed at each frequency and with each amplitude. The average of the 64 measurements was taken as the result. The standard deviation of the 64 measurements is regarded as the measurement error.

A total of 100 chips were measured from a total of 38 100 chips from four production lots. The gamma exposures took about one hour at a dose rate of about 1×10^4 Gy/hr. The same chips were then exposed to the neutron radiation that took about 10 days to reach a fluence of 2×10^{13} cm^{-2}. The ADC parameters were measured before and after the exposure. Table 7 summarizes the results of SNR, WS, and Vref (reference voltage) before the exposure with an input of 450 mV. For comparison, the data sheet values are also listed.

Table 8 lists the changes in SNR after gamma exposure and then after neutron exposure. The comparison is made to the values before the exposure. On average, gamma radiation causes a small degradation in the SNR of about 0.2 dB. The neutron exposure causes mixed changes in the SNR. With a 20 mV input, this change is a 0.03 dB degradation. With a 450 mV input, this change is improved to 0.05 dB. The effect of the changes in the SNR due to gamma exposure are negligible in our application.

Table 8 also lists the changes in WS after the gamma exposure and then after the neutron exposure. The largest degradation of −1.3 dBc is less than the WS variation from chip to chip before exposure (about 3 dBc). Therefore, the gamma and neutron radiation-induced changes in WS are also negligible in our application.

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Table 8. Change in signal to noise ratio (SNR) and worst spur (WS) for the AD9041 after a total ionizing dose of 10 kGy(Si) and a neutron fluence of $2 \times 10^{13}\,\mathrm{cm}^{-2}$.

Input Signal		Average SNR Change (dB)		Average WS Change (dBc)	
Amplitude (mV)	Frequency (MHz)	Gamma Exposure	Neutron Exposure	Gamma Exposure	Neutron Exposure
20	1.25	-0.14 ± 0.01	-0.02 ± 0.01	$+0.50 \pm 0.08$	$+0.05 \pm 0.07$
	2.50	-0.14 ± 0.01	-0.02 ± 0.01	$+0.59 \pm 0.07$	$+0.05 \pm 0.07$
	5.00	-0.12 ± 0.01	-0.03 ± 0.01	$+1.27 \pm 0.07$	-0.24 ± 0.06
	9.60	-0.14 ± 0.01	$+0.00 \pm 0.01$	$+1.01 \pm 0.06$	-0.27 ± 0.06
450	1.25	-0.19 ± 0.02	$+0.05 \pm 0.02$	$+0.82 \pm 0.06$	-1.03 ± 0.07
	2.50	-0.19 ± 0.02	$+0.05 \pm 0.02$	$+0.97 \pm 0.06$	-1.29 ± 0.06
	5.00	-0.21 ± 0.02	$+0.04 \pm 0.02$	-0.12 ± 0.04	-1.15 ± 0.05
	9.60	-0.22 ± 0.01	$+0.06 \pm 0.01$	$+1.01 \pm 0.05$	-1.27 ± 0.05

Vref increased about 1.1% after the gamma exposure but decreased 0.23% after the neutron exposure. It is believed that in real applications where there are both ionizing and NIEL effects, the change in Vref will be smaller than what we have measured. The 1% change in Vref is within the variation of Vref from chip to chip before exposure (table 7), and is within the set selection criteria in the contract.

To conclude, based on the radiation tests of 100 randomly selected chips from 38 100 chips of four production lots, the AD9042 is qualified to be used on the front-end board; no lots were rejected.

5.1.6 Gain Selector

The 12 single-ended TTL digital outputs of the ADC are interfaced to a Gain Selector (GSEL) chip [36]. The GSEL was designed, prototyped, and tested first using DMILL technology. However, when the SCA controller (see section 5.1.9) was developed in the radiation-tolerant DSM process, the opportunity was taken to also target the GSEL design to DSM, using essentially the same Verilog design as for the DMILL GSEL version. The minimum DSM production run was such that the SCA controller, GSEL, and CLKFO chips (see section 5.1.10) were all produced on the same wafers.

The use of the DSM process and radiation-tolerant standard cells leads to sufficient radiation tolerance against TID and NIEL effects. In addition, the GSEL design incorporates features to provide protection against SEU-triggered corruption of the downloaded parameters needed to configure and operate the GSEL. For each of the eight calorimeter channels corresponding to a single ADC, a 32-bit word is assigned in the GSEL to store the relevant parameters. The mapping of these bits includes six Hamming code bits, a 12-bit upper threshold and a 12-bit lower threshold for use in the gain selection algorithm, and two bits which specify the mode in which the GSEL should operate. The six Hamming code bits per 32-bit word are sufficient to provide the following EDAC functionality: if any single bit gets flipped, the error is detected and corrected. If two bits get flipped, the error can be detected, but not corrected. The GSEL was designed such that, for single-bit errors, the data is automatically corrected and an error flag is set in the output data in order to

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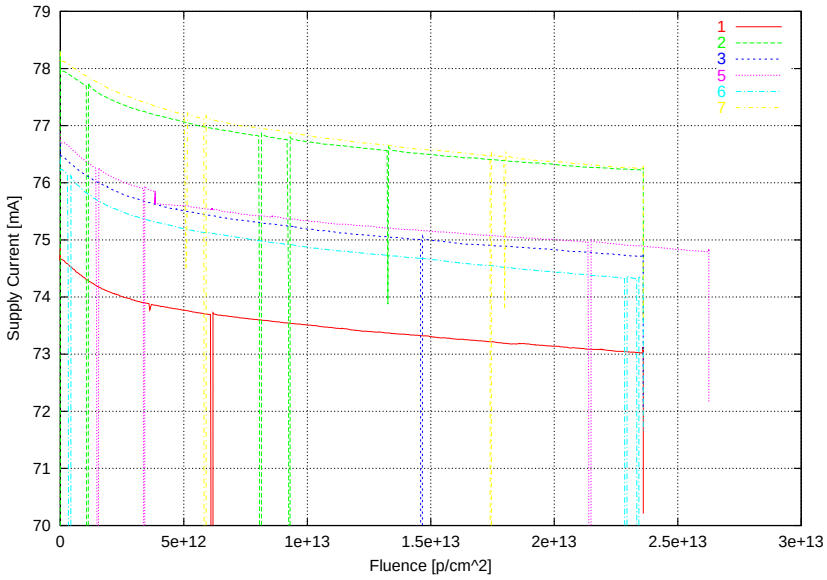

Figure 10. Power-supply current as a function of proton fluence for six DSM gain selector chips from the engineering run.

allow monitoring of the rate of such errors. For double-bit errors, an error flag is set to indicate the need to download the parameters again in order to fix the problem. A total of five mode bits is sufficient to fully specify the GSEL operation, while 16 mode bits are available, distributed over the eight 32-bit channel words. The mode bits are even more protected against SEE by distributing three redundant copies of the five mode bits over the eight words, and using majority-voting logic to set the selected mode.

A number of both DMILL and DSM GSEL chips were subjected to a proton flux of energy 158 MeV. Details of the test results with prototype chips can be found in ref. [36]. Here we summarize the results of testing six DSM GSEL chips from the pre-production, or so-called, engineering run [37]. The current drawn by the DSM GSEL was monitored during exposure. As the integrated dose increased, the current exhibited a slight decrease; the current versus proton fluence is shown in figure 10. Similar behaviour was observed in the chips from the prototype runs, as well as in other chips produced with the same DSM process (for example, see ref. [38], where it has been attributed to an increase in absolute value of the threshold voltages of both the n-channel and p-channel transistors). This very small effect is of no concern for operation in ATLAS. Apart from this gradual and steady decrease in current, the voltages and currents of all samples were stable during exposure. No occurrence of latch-up was observed. During the test, the chips were operated as they would be on the front-end board, thus the dips in figure 10 are where SEUs occurred, and the logic was stopped, reset, and restarted.

During the exposure, some logic errors were observed. Summing over all exposed samples, a total of 16 SEU were observed from a total proton fluence of 1.6×10^{14} cm^{-2}, yielding an SEU cross-section of 1×10^{-13} cm^2. This value is approximately an order of magnitude lower than the value of 1.2×10^{-12} cm^2 determined for the DMILL version of the GSEL, which was derived from the same Verilog code and therefore had the same logic design.

Since a total of 896 front-end boards are required to instrument the full electromagnetic bar-

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rel calorimeter and each front-end board contains eight GSEL chips, the electromagnetic barrel readout includes a total of 7 168 GSEL chips. The measured SEU cross-section implies a total of 8 830 SEUs per 10 years of LHC operation at design luminosity, including a safety factor of 10. Assuming 10^7 s of LHC operation per year, this corresponds to a mean time between SEUs in the electromagnetic barrel calorimeter readout of five hours. This very low rate is a conservative estimate, since most of the errors are automatically corrected via the redundant storage and SEU protection of the GSEL design, and we have applied the measured cross-section for 158 MeV protons to all hadrons above an energy of 20 MeV.

5.1.7 Output optical link

The digitized data are sent off the detector away from the radiation environment through digital optical links to the digital-processing units some 100 to 200 meters away. When an event is triggered, five samples around the signal peak are converted to digital format by a 12-bit ADC clocked at 5 MHz. There are 16 ADC chips on one front-end board and each ADC chip digitizes signals from eight detector channels. Four bits are added to the 12-bit ADC output to form a 16-bit event word. These four bits have two gain bits, one odd parity bit, and one bit that is permanently set to zero. To avoid sending these 16-bit data from 16 ADC chips across the front-end board to the input of the optical link, each 16-bit 5 MHz word is multiplexed down to 2-bit 40 MHz data words, and converted into PECL differential data format. These 2-bit words from each ADC are then transmitted to the input of the optical link, forming a 32-bit word at 40 MHz.

Located at about the centre of the outer edge of the front-end board, the optical link receives this 32-bit word at 40 MHz and converts it into a 1.6 Gbps serial data stream with transmission protocol. This serial data stream is further converted from an electrical signal to optical, and transmitted to the back-end electronics through one optical fiber. The optics breaks the ground loop between the front-end and the back-end electronics, and a single fiber reduces the link medium material. The transmitting part of the optical link is located on the front-end board and is subjected to radiation. This part of the link begins with an ASIC called SMUX [39, 40]. The output of SMUX is connected to a COTS serializer chip called the GLink. The output of the GLink is in PECL differential data format. An electrical to optical signal converter converts this PECL signal into an optical signal at an 850 nm wavelength and launches it into an optical fiber. This converter is a subassembly made of a COTS laser driver chip (SY88922V from Micrel Inc.) and a VCSEL (TTR-1A43 from TrueLight Corp.) housed in the industrial standard ST optical package. This subassembly is named OTx. The fiber that connects the OTx to the back-end receiver is a germanium doped graded index and multimode fiber with a 50 micron core and 125 micron cladding. The fiber is produced by Plasma Optical Fibres (now Draka) and packaged into cables by Ericson.

SMUX is an ASIC chip developed in the DMILL technology. SMUX converts the 32-bit parallel data in PECL to 16-bit in TTL to match the GLink input. SMUX chips from production batches were exposed to check for TID and NIEL effects, and to measure the SEE induced error rates. Six SMUX chips were exposed to a ^{60}Co gamma-ray source. No errors were observed after the chips received a total dose of 15 kGy, more than 12 times the total dose required for production qualification. Six SMUX chips were exposed to neutrons ranging from 3 MeV to 30 MeV to check for NIEL effects and measure SEE error rates. No malfunctions were observed after exposure to a neutron fluence of 3×10^{14} cm^{-2} (1-MeV neutron equivalent in Si), about nine times the fluence

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required for NIEL and 47 times the fluence required for SEE production qualification. Tests of SEE were also carried out with protons ranging from 20 MeV to 160 MeV. Two SMUX chips were exposed to a proton fluence of 1.2×10^{12} cm^{-2}. No hard destructive SEE were observed in either the neutron or proton exposures. The soft SEE error rate was convoluted with the simulated ATLAS neutron energy spectrum to estimate the SEE error rate in the ATLAS environment. The soft SEE error rate is estimated to be below 0.1% of that from the GLink.

The GLink (HDMP-1022/1024 from Agilent Tech.) is a serializer and de-serializer chipset based on silicon bipolar technology. The transmitter chip (HDMP-1022) serializes the 16-bit 80 MHz TTL input parallel data into a 1.6 Gbps serial bit stream. The receiver chip (HDMP-1024) de-serializes this serial bit stream and recovers the 16-bit 80 MHz TTL parallel data and the clock. We carried out extensive radiation tests on the HDMP-1022. Our final qualification tests were carried out with chips produced by Agilent Technologies.

TID effects were checked with gamma rays from ^{60}Co sources at various locations including BNL. In these tests, links with the GLink and optical channel (optical transmitter and receiver with the fiber) were operated with the transmitting part (HDMP-1022, OTx and a section of the fiber) exposed to radiation. The bit error rate was monitored before, during, and after the exposures. With 12 links in the test, there were no errors during an exposure period of more than 24 hours and a total dose of 43 kGy, more than five times the required total dose. The NIEL and SEE tests were performed on more than 20 links with neutron (maximum energy of 25 MeV) and proton (energy of 200 MeV) beams with fluences of 4.8×10^{14} cm^{-2} (1-MeV neutron equivalent in Si) and 2.8×10^{13} cm^{-2} respectively, more than twice the required fluences. No latch-up was observed. Detailed studies on the SEU error rate under neutron exposure have been published [41]. In that test, we measured a neutron-induced SEU energy threshold of 2.5 MeV. We used the "Burst Generation Rate" (BGR) model [42] to analyze the data and found that this energy threshold came from the two interactions: n + ^{28}Si $\rightarrow$ p + ^{28}Al and n + ^{28}Si $\rightarrow \alpha$ + ^{25}Mg. The recoiling ions caused the bit-flip errors. The estimated error rate per link in ATLAS operation is 0.065 per hour. This error rate comes from the GLink and the OTx, and it generates a link system deadtime that is below the average deadtime of the overall electronics system, so it is acceptable. During the above tests, the OTx was also tested. When the GLink was shielded from radiation exposure, the SEU error rate from the OTx was found to be about 1% of that when the GLink was not shielded. This indicates that the SEU errors were mostly generated in the GLink.

The optical link serial data rate of 1.6 Gbps requires graded index fiber. In our design of the optical link, we choose an optical power margin of 10 dB between the OTx and the optical receiver assembly (ORx). Taking into account the optical power loss from the fiber and connectors at the OTx and ORx, and at several patch panels, we assigned a limit for the radiation-induced optical power loss in the fiber to be less than 0.1 dB/m. There is no ATLAS wide policy for qualifying fibers. We used the radiation requirement for electronics at the front-end board location. This resulted in a total dose requirement of 2.8 kGy for the production qualification of the fiber. Germanium doped fiber from Plasma Optical Fibres was found to have a radiation induced attenuation within this limit [43]. In the pre-selection stage, these fibers have been shown to withstand doses over 800 Gy(Si) and 2×10^{13} cm^{-2} (1-MeV neutron equivalent in Si) with less than 0.1 dB/m attenuation. The fiber batch used for the production of the optical cables was qualified using a ^{60}Co source. Two 5 cm diameter rolls with 100 m of fiber each were exposed at a dose rate of 150 Gy/hr.

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After one hour of exposure, the transmission loss over the 100 m was less than 10%, or less than -0.005 dB/m. Immediately after two hours of exposure (300 Gy) the loss was -0.04 dB/m, but it improved to -0.015 dB/m within 10 minutes, indicating a fast annealing process was taking place. The optical loss was measured to be -0.135 dB/m immediately after the total dose reached 2.8 kGy. Within one hour of annealing at room temperature, the loss was reduced to -0.1 dB/m, satisfying the requirement set. We expect the actual loss in the ATLAS environment will be less than -0.1 dB/m due to the fast annealing process. Because there are only a few meters of fiber actually at the front-end board location, we estimate a maximum optical power loss due to radiation to be less than 1 dB, well within the 10 dB power margin.

5.1.8 SCA control bus

The SCA control bus is driven using commercial MC10H116D ECL triple-line receiver chips. Radiation tests with samples were performed to verify the radiation tolerance of these devices. For the final production front-end boards, negotiations with ON Semiconductor and a distributor culminated in an agreement wherein we ordered the full quantity of more than 18 000 MC10H116D parts required from a single existing production lot. As a first stage in the procurement process, we received 50 samples from this reserved lot for radiation testing. The agreement stipulated that, in the event that the devices did not pass our radiation-tolerance requirements, we could cancel the order without penalty. Once the radiation tests were successfully completed, we proceeded with the complete order and purchased all of the production parts.

Various groups within ATLAS expressed interest in using MC10H116 chips, namely on the liquid argon calorimeter controller board and in the muon system Cathode Strip Chambers (CSC) readout. We agreed to purchase sufficient MC10H116 chips from our production lot for these applications as well, and to perform the radiation qualification tests of the production lot such that it satisfied the requirements of all three applications. The liquid argon calorimeter controller board resides in the same crates as the liquid argon front-end boards, and therefore has identical radiation-tolerance criteria (see section 5.4). However, the expected neutron level in the worst case position of the CSC readout is a factor of about 3.4 higher than for the liquid argon calorimeter readout. We therefore exposed a subset of the production chips to these higher levels in order to satisfy this criterion.

A test jig was designed to allow AC measurements during exposure, in addition to online current and voltage measurements. All three of the line receivers of the device under test could be driven with a differential clock signal, and one of three differential outputs could be observed. The input and output differential signals were transmitted over about 50 m of coaxial cable installed between the control room and the cyclotron vault. During exposure, we used an external pulse generator to send a 40 MHz differential clock signal of about 400 mV amplitude to the MC10H116 inputs. The MC10H116 output signal was recorded using a digital oscilloscope, which displayed the received signal and also measured the voltage levels, and rise and fall times.

Sixteen parts were exposed to a proton fluence of 9.2×10^{12} cm^{-2}, by which point they exceed the required TID and SEE levels by very large factors. Due to the higher NIEL radiation-tolerance criterion of 2.7×10^{13} cm^{-2} (1-MeV neutron equivalent in Si) for the CSC readout, an additional 12 parts were later exposed to fluences which met or slightly exceeded this tolerance level.

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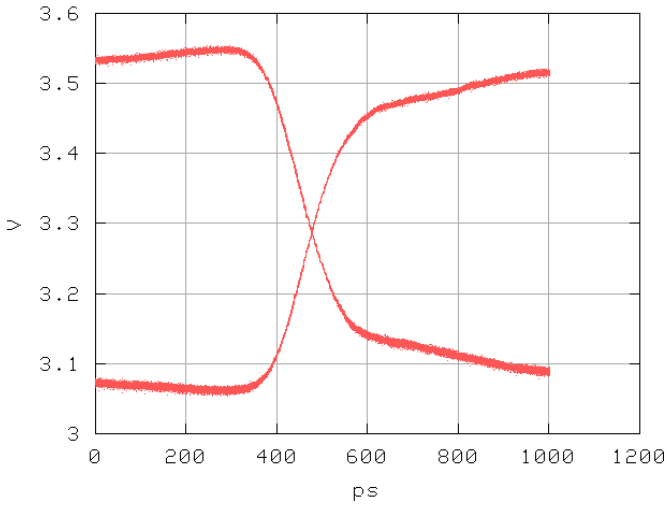

Figure 11. Measured output pulse shape accumulated during exposure of a MC10H116D production sample with the oscilloscope set to infinite persistence.

No significant variations in the voltage levels, or rise and fall times of the MC10H116D output signal were observed. As an example, figure 11 displays the pulse shape accumulated during exposure of one production MC10H116D sample with the oscilloscope configured to infinite persistence. No occurrence of latch-up was observed. The devices, powered with a 5 V supply, had a typical current before exposure of approximately 82 mA. A slight change in the current with fluence was observed, amounting to less than 1 mA. This very small effect is of no consequence for operation in ATLAS. More details of the radiation tests can be found in ref. [44].

5.1.9 SCA Controller

The SCA controller (SCAC) ASIC provides the main digital control of the front-end board. The SCAC receives the trigger information and generates the write and read addresses for the SCA pipelines. In addition, the SCAC controls the flow of the SCA readout via its communication with the GSEL.

The SCAC contain a large amount of dual-ported SRAM, which poses its own unique radiation-tolerance problem. Seven FIFOs and three dual-ported RAM are used for a total of nearly 3 300 RAM bits [45, 46]. In addition to the SRAM, the SCAC contains 957 D-flip-flops, including those embedded inside the SRAM blocks. With few exceptions, all I/O to and from the SCAC uses LVDS levels, with differential receivers on all input pairs and current mode LVDS drivers on the output pairs.

Due to SEU issues observed in FPGAs, the SCAC design was implemented in an ASIC using both radiation-hard DMILL technology and commercial DSM CMOS technology. In addition, SRAM using radiation-tolerant latch cells in DMILL technology was developed and submitted for fabrication. Based on risk, cost, speed, and radiation tolerance, the DSM technology was chosen for fabrication. DSM SCAC prototypes were fabricated in two multiproject wafer (MPW) runs to test the functionality, speed, and radiation tolerance. With the success of the MPW prototype, this

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circuit, along with circuits for three other devices were submitted as a dedicated engineering run to produce two wafers. The die size was 4 mm $\times$ 4 mm.

A detailed description of the radiation tests of the SCAC have been published [38]. Here we only provide a summary. To test the radiation tolerance, a number of prototype SCAC chips have been exposed to X-rays, protons, and neutrons. The predominant effect for digital CMOS electronics due to ionizing radiation is leakage currents in transistors. The maximum drop in current from X-rays was 4.2 mA, or 3.4%, from a dose of 44 kGy(SiO_2) or over 75 times the radiation tolerance criterion for qualification. The maximum drop in current from protons with energy of 159 MeV was 2.0 mA, or 1.8%, from a dose of 18 kGy(SiO_2) or over 30 times the radiation tolerance criterion for qualification. We estimated the current will drop about 20 μA, or 0.02%, during the 10 years of operation in ATLAS. This small decrease in current will have negligible effect on the operation of ATLAS.

Ten SCAC chips were exposed to neutrons to a fluence of $(1.9 \pm 0.4) \times 10^{13}\,\mathrm{cm}^{-2}$ (1-MeV neutron equivalent in Si). This is 12% above the radiation tolerance criterion for qualification, although NIEL qualification of the SCAC in DSM CMOS was not necessary. In addition, 26 parts have been exposed to protons of fluences giving at least two times higher damage than the equivalent 1-MeV neutron fluence anticipated from 10 years of ATLAS operation. All parts functioned correctly after exposure.

The SCAC may be affected by soft nondestructive single-event effects, such as single-event upsets, transients, or functional interrupts. The analysis of the upsets is complicated by the considerable circuit-mitigation techniques that are employed in the SCAC design [38]. The FIFO memories within the SCAC are made with SRAM, which are protected by EDAC units at three different locations. All single-bit upsets in the SRAM are corrected in real time. They have no consequence on the operation of the SCAC but are recorded.

Multiple-bit upsets in the SRAM are possible and are not corrected by the EDAC logic. However, these types of upsets are detected and recorded. Since multiple-bit upsets cannot be automatically corrected by the EDAC logic, their occurrence will require that the front-end board with the affected SCAC be reset in order to resynchronize the data flow.

Upsets in critical bits in the SRAM, the registers, and some combinatorial logic are protected by using triple-redundant majority-voting logic. Upsets in these parts of the circuit will be corrected and have no effect on the operation.

The energy and angular dependence of the proton-induced upset cross-sections have been measured and are shown in figures 12 and 13. No occurrence of a hard destructive SEE, such as single-event latch-up, has ever been observed. The total upset cross-section is dominated by the SEU occurring in the SRAM. The threshold energy was approximately 110 MeV and the saturation cross-section was $3 \times 10^{-11}\,\mathrm{cm}^2$ for all upsets. The threshold energy was approximately 140 MeV and the saturation cross-section was $2 \times 10^{-12}\,\mathrm{cm}^2$ for single-event functional interrupts.

The frequency of occurrence of each type of upset in ATLAS was estimated by convolving the fitted upset distributions with the simulated energy spectra for neutrons, pions, and protons at the location of the SCAC chips in the ATLAS detector. The predicted upset rates were scaled to the entire system of 1 792 SCAC chips required to read out the electromagnetic barrel liquid argon calorimeter. The measured upset rates imply the mean time between correctable SRAM upsets will

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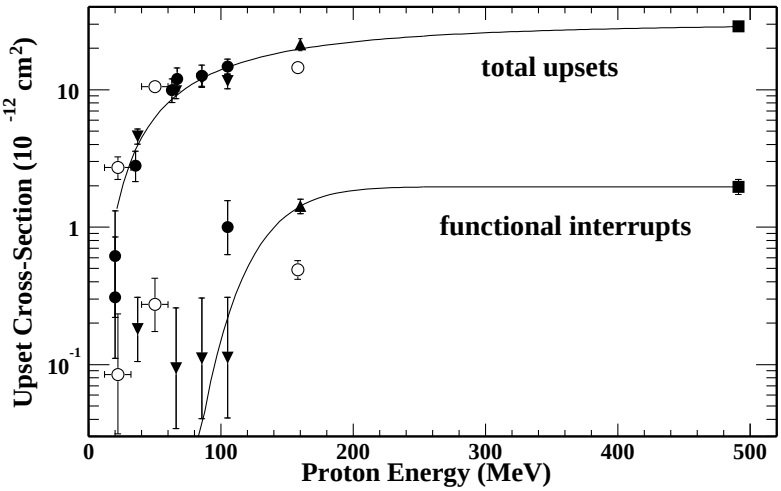

Figure 12. Proton-induced upset cross-sections for the switched capacitor array controller: total upset (upper data) and single-event functional interrupts (lower data). The solid circles and inverted triangles are data taken with the 2C beam line at TRIUMF, the solid squares are data taken with the 1B beam line at TRIUMF, the solid triangles are data taken with the Northeast Proton Therapy Center at Massachusetts General Hospital, and the open circles are data taken at Harvard Cyclotron Laboratory. The open-circle data is not included in the fits. For each energy there are two data points; the upper point of a given marker type is the total number upsets and the lower point of a given marker type is the number of functional interrupts [38].

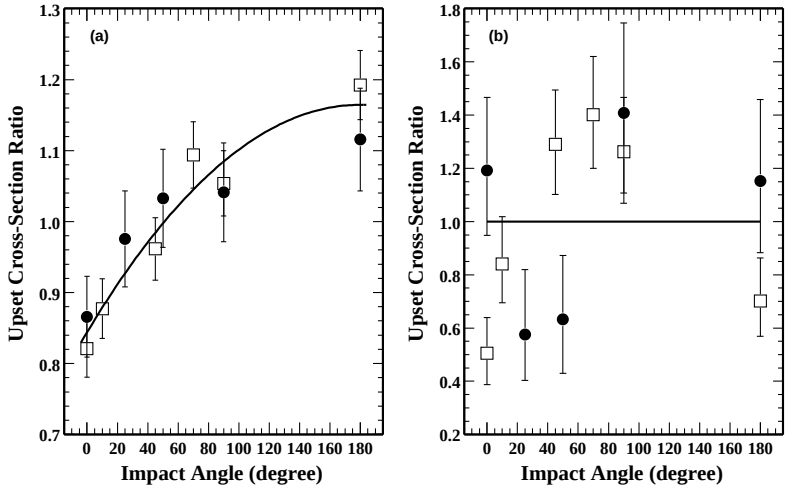

Figure 13. Ratio of the proton-induced upset cross-section at impact angle θ to the cross-section averaged over all angles for the switched capacitor array controller: (a) SRAM single-bit upsets and (b) single-event functional interrupts. The solid circles are for engineering prototype parts exposed to a proton beam energy of 159 MeV, while the open squares are for MPW prototype parts exposed to a proton beam energy of 491 MeV [38].

be two days and the mean time between upsets that require a reset to be 50 days. These rates are very low and perfectly manageable for ATLAS operation.

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5.1.10 Clock distribution

The input clock is recovered on the front-end board from the input TTC signal, via the on-board TTCrx chip [47]. All clocks on the front-end board are derived from this single input 40 MHz clock. The TTCrx includes an on-chip phase-locked-loop circuit with a wide lock range, but provides a recovered clock with rather large random and TTC data-dependent jitter. The jitter levels are too high to provide stable operation of the output optical link. To solve this problem, the front-end board design was modified to include a QPLL chip. The QPLL is a phase-locked-loop based on a voltage-controller quartz crystal oscillator developed as a jitter filter for the TTCrx clock and implemented in the DSM process [48].

The QPLL output clock feeds a clock fanout tree for the entire front-end board, which is comprised of custom CLKFO chips. The CLKFO ASIC was developed to provide several functions needed in the front-end board clock distribution. The CLKFO receives as inputs two LVDS clock signals, denoted CLK1 and CLK2. The CLK2 signal is clipped such that the high phase of the clock is approximately 6 ns. Two identical copies of the clipped CLK2 differential signal are output. The differential CLK1 input is fanned out internally to provide three single-ended TTL output copies. In addition, the CLKFO has eight LVDS outputs related to CLK1. Depending on whether one of the CLKFO pins is tied high or low, the LVDS outputs are either eight identical copies of CLK1, or four copies of CLK1 and four identical 5 MHz signals, that are derived by counting down the CLK1 40 MHz signal. The down-counter for generating the 5 MHz signal is designed using triple-redundant counters and majority-voting logic to harden the design against SEUs.

A number of CLKFO and QPLL chips were subjected to radiation testing using 158 MeV protons [37, 49]. Here we summarize the results of testing six CLKFO chips from the engineering run. During the exposure, an external pulse generator was used to send a 40 MHz differential clock signal to the input of the CLKFO, and one of the CLKFO output signals was observed on an oscilloscope. Depending on jumper settings on the test jig, the observed output could be either the clipped output clock signal or the signal generated by the 5 MHz down-counter. The input and output differential signals were transmitted over about 100 m coaxial cables installed between the control room and the cyclotron vault. The test jig allowed the current drawn by the CLKFO to be monitored online. As for the other DSM chips and as discussed previously, a small decrease in current was observed with increasing proton fluence. This effect is of no concern for operation in ATLAS. During monitoring of the 5 MHz output, performed for three of the chips, no SEU of the triple-redundant down-counter was observed. No occurrence of latch-up was observed.

Seven QPLL and crystals oscillators were exposed to 158 MeV protons up to a fluence of 2.5×10^{13} cm^{-2}. No latch-up was observed. One, possibly two, SEUs were observed from which the QPLL recovered without external intervention. The upper and lower limits of the frequency lock range decreased after exposure, which is understood to be due to ionizing radiation. However, the circuit was always able to lock on the nominal LHC frequency. The measurements were not sensitive to possible upsets in the QPLL output frequency divide/counters.

5.1.11 Control interfaces

Run parameters are downloaded to the front-end boards over a serial bus running along the front of each front-end crate in the system. The read back of the parameters and monitoring data flows

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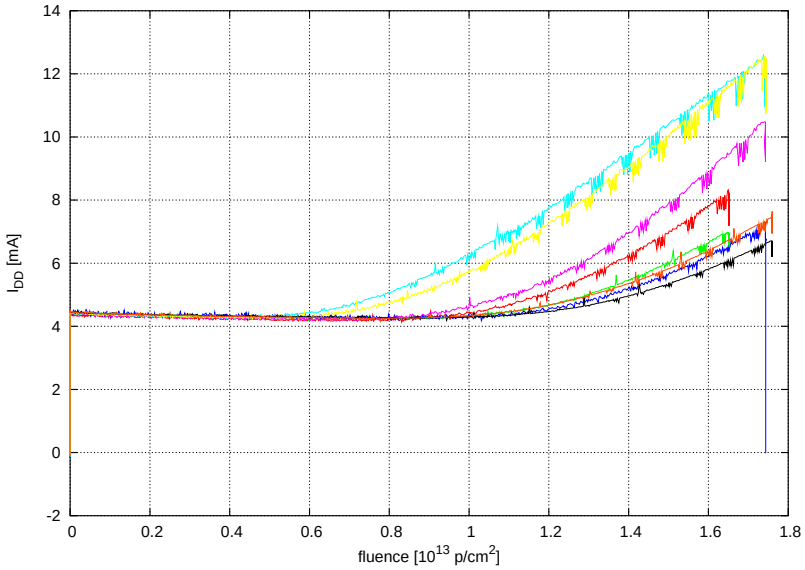

Figure 14. Power-supply current as a function of 158 MeV proton fluence for eight configuration controller ASICs.

in the reverse direction on the same serial bus. Each front-end board has an on-board SPAC (Serial Protocol for the ATLAS Calorimeters) slave ASIC [50] to allow configuration and monitoring of the front-end board via the SPAC bus. Most of the front-end board configuration is performed via the parallel bus of the SPAC slave, which is connected to the configuration controller chip (CONFIG) [51]. The exceptions are the use of the SPAC slave I2C ports connected to the TTCrx and to the two DCU temperature and voltage monitoring chips [52]. The CONFIG is responsible for writing and reading the information to and from the configuration memories of the ASICs on the front-end board. It communicates through different protocols to the gain selectors, the SCA controllers, the shapers, and the voltage regulators.

The CONFIG chip is realized as a DMILL ASIC. As described in more detail in ref. [53], a number of CONFIG chips were subject to radiation testing using a 158 MeV proton beam. The supply currents of all samples were monitored during exposure. No occurrence of latch-up was observed. The supply current versus proton fluence is shown in figure 14 for eight devices. The devices showed an increase in supply current with exposure. Similar behaviour was seen in radiation tests of DMILL GSEL chips produced as part of the same MPW run. Since the total GSEL current is much larger than for the CONFIG current, but the absolute increase was similar, it is believed the current increase is probably in the differential receiver cells, of which the CONFIG has four and the GSEL five. The same receiver cells are used in the SCA, where no such current increase was observed. It is possible, therefore, that the increase resulted from some feature of the processing of this particular MPW, and will not be observed for chips from the final production run. In any case, the effect is so small that it would have a negligible impact on operation in ATLAS and poses no concern, so we did not repeat the testing with production chips.

During the exposure of these eight CONFIG chips, the monitoring looked for SEUs. A total of nine such upsets were observed, with a 158 MeV proton total fluence of $1.38 \times 10^{14}\,\mathrm{cm}^{-2}$, corresponding to an SEU cross-section of $6.5 \times 10^{-14}\,\mathrm{cm}^2$. A total of 896 front-end boards are

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required to instrument the full electromagnetic barrel and each front-end board contains a single CONFIG. The measured SEU cross-section implies a total of approximately 450 SEUs per 10 years of LHC operation at design luminosity, including a safety factor of 10. Assuming 10^7 s of LHC operation per year, this corresponds to an SEU-induced error in the electromagnetic barrel readout every three days. Even this very low rate is a conservative estimate, since during data taking the SPAC system, and therefore the CONFIG, is idle most of the time.

5.1.12 Voltage regulators

Voltage regulators are used on the front-end board to reduce the sensitivity to power-supply noise and provide current limiting, as well as a thermal shutdown function in case of over-heating. Since the front-end board voltage regulators are equipped with an inhibit control pin, they can be switched on and off remotely. Thus the possibility exists to power cycle a component, without having to power off the entire crate, such as if a radiation-induced latch-up condition is encountered. Positive and negative regulators are used. Several commercial voltage regulators were exposed to radiation. None of them survived and therefore we did not used them. ST voltage regulators were eventually used [54].

A total of 12 negative-voltage regulators (LHC7913) were exposed to 158 MeV protons up to a fluence of $2.5 \times 10^{13}\,\mathrm{cm}^{-2}$. Half of the samples were connected with $V_{\mathrm{out}} \simeq -3\,\mathrm{V}$ and the other half with $-1.78\,\mathrm{V}$; typical load currents were about 0.5 A to 0.7 A. None of the 12 samples died during exposure. The positive-voltage regulators (LHC4913) have been extensively radiation tested [55]. They are stable during exposure to radiation.

5.2 Level-1 trigger summing

A trigger decision is based on the energy contained in a group of calorimeter cells pointing to the interaction region. To compute this energy one needs to sum the charge in a group of channels (trigger tower). Trigger towers are formed by analog summing signals from four longitudinal segments in the same η-ϕ location. For the electromagnetic barrel calorimeter, analog sums are formed at three stages: in the linear mixer of the shaper chip (see section 5.1.3), the layer sum board (see section 5.2.1), and the tower builder board (see section 5.2.2).

In the case of the hadronic end-cap calorimeter, this summing is performed by the linear mixer of the shaper chip and special types of layer sum daughterboards on the front-end board; no further summation of the signals is necessary for the level-1 trigger system. Thus a special board was needed to replace the tower builder board. This board is referred to as the tower driver board. Since no summation is implemented, the function of this board is to produce differential signals and to drive 70 m of trigger cables. In the case of the forward calorimeter, the trigger towers are formed by two steps of summing, both in the linear mixer and in the layer sum board. Since no further summation is needed, the tower driver board is also used for this calorimeter subsystem.

5.2.1 Layer sum board

The ATLAS liquid argon calorimeter signals are summed to make trigger towers. The trigger sums are formed using analog techniques. The shaper contains a linear mixer, which forms the sum of the four calorimeter signals processed by the chip. On the front-end board, the sum of the outputs

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of the linear mixers, which belong to the same trigger tower, are made on the layer sum board [56]. The number of inputs to sum depends on the section of the calorimeter involved. Different types of layer sum boards are used on the front-end boards to service different depth layers.

The layer sum board is a small daughterboard which resides on either side of the front-end board and thus it is necessary to test these boards for their tolerance to radiation. A voltage-limiting operational amplifier (HFA1135) was chosen as the summing amplifier. Only ceramic bypass capacitors were used, since tantalum capacitors are known to be radiation sensitive. The version with 16 HFA1135 operational amplifiers arranged as eight two-stage amplifiers ($S2 \times 8$) was chosen for radiation tests.

To carry out the tests, a small fixture was built on which four layer sum boards could be mounted, one behind the other, separated by a distance of approximately 10 mm. A set of $S2 \times 8$ layer sum boards were exposed to approximately 1 MeV neutrons at Lowell, and a second set were exposed to gamma rays using a ^{60}Co source at BNL. A third set of boards were exposed to neutrons of up to 20 MeV at CERI to test for SEE. The fluence of neutrons achieved for different amplifiers varied between $1.0 \times 10^{13}\,\mathrm{cm}^{-2}$ and $3.0 \times 10^{13}\,\mathrm{cm}^{-2}$, the variation being due to the spatial inhomogeneity of the radiation source. For the gamma-ray exposures, the boards were removed sequentially from the source, resulting in different radiation doses for each board. The doses achieved were approximately 0.87, 2.50, 4.65, and 8.70 kGy. The boards were powered during both exposures, and there was no significant variation in power consumption during either test. At CERI, eight un-powered layer sum boards were exposed to neutrons up to a fluence of $3.0 \times 10^{13}\,\mathrm{cm}^{-2}$ and one powered board was exposed to a fluence of $2.5 \times 10^{13}\,\mathrm{cm}^{-2}$. The powered board was operated as an eight-channel amplifier of low frequency (1 kHz) sine waves and monitored manually. No channels on this board were observed to fail during the exposure. After exposure, a set of performance histograms were made for each board.

The HFA1135 is a fast bipolar operational amplifier and it is expected to be reasonably insensitive to radiation. Our tests confirm this expectation, as the only significant effects that we observed were a change in both the breakpoint voltage and the slope of the saturation curve. The breakpoint voltage is an experimental parameter defined in ref. [56], which indicates the point at which voltage limiting sets in. The difference between response curves before and after receiving a neutron fluence of $3.0 \times 10^{13}\,\mathrm{cm}^{-2}$ was small. Figure 15 shows a plot of the breakpoint voltage as a function of neutron fluence (for the low-energy neutron exposure). The effect of radiation on this parameter is clearly visible, but the magnitude of the change is acceptable. Changes were only seen for the neutron exposure.

On the basis of the results of the low-energy neutron exposures, we decided to raise the reference voltage from ± 3.3 V to ± 3.6 V, to insure that the clamp voltage remains well above 3.0 V, and to compensate for possible effects of radiation as the layer sum boards age.

5.2.2 Tower builder board

On the tower builder board [57], it was necessary to radiation qualify the three COTS operational amplifiers HFA1135, AD8001, and AD8011 [58]. In addition, since a CMOS analog switch failed after about 100 Gy, independent of dose rate, an ASIC was developed in DMILL technology, BIMUX.

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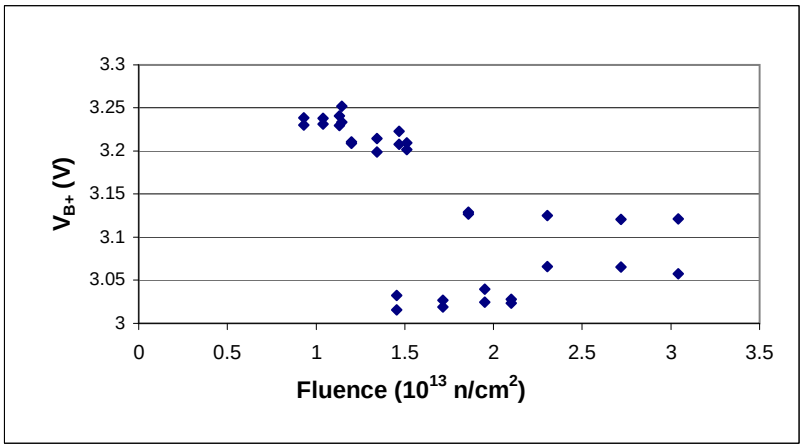

Figure 15. Variation in the upper breakpoint voltage of the $S2 \times 8$ layer sum board versus fluence for low-energy (approximately 1 MeV) neutrons.

Three radiation sources were used for the pre-selection tests of the components on the tower builder board. TID testing was performed using a ^{60}Co source at Pagure. The chips received a total ionizing dose of 3.5 kGy at a rate of 160 Gy/hr. NIEL testing was performed using a neutron source at the ULYSSE (subcritical reactor). The neutron fluence (1-MeV neutron equivalent in Si) was 1.1×10^{13} cm^{-2} during one exposure and 3.2×10^{13} cm^{-2} during a second exposure. SEE testing was performed using a 60 MeV proton source at Louvain la Neuve. The proton fluence received by each board was 3×10^{13} cm^{-2} .

For the pre-selection tests, measurements were made using a test setup that measured, as a function of flux: gain, output offset, output peaking time, output noise, power-supply current, latch-up, and SEU. The BIMUX chip and three operational amplifiers did not show significant modifications of electrical characteristics after the gamma-ray and neutron exposures. Four BIMUX chips were exposed to protons such that eight registers were exposed. Based on no SEE after a proton fluence of 3×10^{13} cm^{-2}, we estimated at most one SEU in the full ATLAS experiment every eight days. No occurrence of latch-up was observed.

For the radiation qualification tests, the BIMUX chip was not required to be radiation qualified since it used DMILL technology. However, the three operational amplifiers, HFA1135, AD8001, and AD8011, were required to pass radiation qualification tests against latch-up. For these tests, samples were taken from each batch of production amplifiers.

Two special test boards were developed to perform the qualification test. These boards have the same printed circuit, but different components. The first board contained 90 operational amplifiers: 10 samples from each of nine batches (two AD8001, one HFA1135, and six AD8011). The amplifier layout shape was circular to fit the beam shape. This board was put perpendicular to the beam line. The second board contained one LED per operational amplifier (see figure 16). An LED went on when a latch-up occurred in the corresponding operational amplifier of the first board. The second board was put in the control room with the power supply. The 90 samples were exposed to protons at Louvain la Neuve to a fluence of 1.18×10^{13} cm^{-2} after 6 hr and 15 min. No latch-up was observed.

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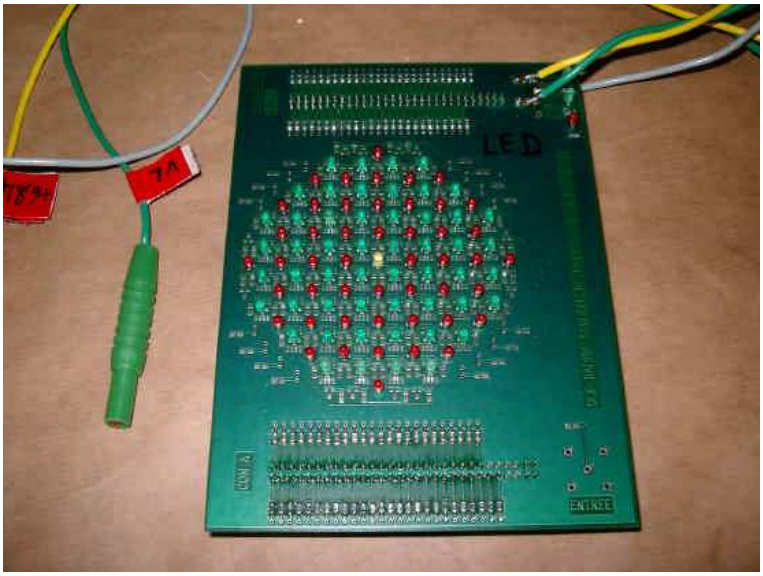

Figure 16. LED board for the radiation qualification of the tower builder board.

5.2.3 Tower driver board

The tower driver board [59] is placed in the end-cap front-end crate. There is only one active component on the tower driver board, the AD8001 fast-bipolar operational amplifier. These amplifiers have been tested for the tower builder board and pre-selection tests gave satisfactory results. The accumulated neutron and gamma-ray doses were both much higher than needed for the tower driver board radiation-tolerance criterion. Other components on the board are chip resistors and ceramic capacitors with know radiation tolerance.

5.3 Calibration board

The calibration board transmits well-defined pulses to the motherboards or preamplifiers to enable the response of the electronics to be characterized. There are about a total of 9 000 components on each side of the board, including 64 pulsers.

The sensitivity to radiation of the various COTS on the calibration board has been evaluated. All components were found to be tolerant enough except for a voltage regulator (LM337), operational amplifier (OP07), and DAC. The voltage regulators were not essential and were replaced by diodes. A static low-offset operational amplifier and ladder DAC have been designed in DMILL technology [60]. In addition, there are some digital control functions on the calibration board. A radiation-tolerant digital ASIC was developed to handle these functions.

In order to cope with the ATLAS liquid argon calorimeter dynamic range, a DAC with at least 16-bit was used on each calibration board. The DAC is an array of 16 identical switched current sources (1 mA) driven by a common reference source and connected to a 0.1% precision $R/2R$ network with resistance values selected by giving the needed voltage swing. This architecture guarantees an excellent monotonicity and good linearity [60].

First a DAC was developed which was not specifically designed for radiation tolerance. The offset drifted by a few mV after a neutron fluence of 10^{11} cm^{-2} and the DAC died quickly after a

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few krad of total ionizing dose. To meet the radiation-tolerance requirements, the DAC was custom designed in DMILL technology. The performance of the DMILL version was adequate under neutron and proton exposures. A small drift of the DAC output voltage was observed under gamma-ray exposure and was tracked to a change in reference current. As a consequence, a new reference current source was incorporated; the current mirror, which drifted under exposure, was replaced by a reference source built around the low-offset operational amplifier that was also developed.

The low-offset operational amplifier is the key element needed to build the 128 precision DC current sources on the calibration board. It is also used to distribute the DAC voltage throughout the board with minimal voltage drop. The voltage to current conversion uses the low-offset operational amplifier and a 0.1% 5 Ω external resistor.

No commercial operational amplifier that we tested under radiation fulfilled our requirements, so two different approaches were tried: a CMOS auto-zero operational amplifier, and a bipolor static low-offset operational amplifier with external precision components and fuses to trim down the offset to the specified accuracy. The performance of these two designs in 0.8 μm BiCMOS and the relative ease of implementation of the digital part lead to the choice of static operational amplifier. This low-offset operational amplifier design was migrated to a DMILL ASIC, and performed as expected.

The first version of the chip was tested under gamma-ray radiation (^{60}Co) and the output current was monitored for different inputs. No effect was observed after three times the TID radiation-tolerance criterion. These chips were then tested with 10 MeV neutrons up to a fluence of 9×10^{13} cm^{-2}, far in excess of the NIEL radiation-tolerance criterion. After a neutron fluence of 2.3×10^{13} cm^{-2}, the circuits could no longer be measured online because of the failure of a discrete NPN transistor used in the testing control circuit. The offsets of the circuits were measured again after exposure and found to be only 50 μV for a chip exposed to the maximum fluence.

To control and load parameters to the calibration board, an ASIC named CALOGIC was developed in DMILL technology. The CALOGIC ASIC needed to be tested not only for NIEL and TID effects, as for the DAC and low-offset operational amplifier, but also for SEE. The SEE test was performed at Louvain la Neuve using a 60 MeV proton beam with a flux of 4×10^8 cm^{-2}s^{-1}. This test was performed on four CALOGIC chips during 10 hours. The main goals were to check for possible SEE in the I2C 32-bit register and to monitor the power-on-reset delay. The setup allowed the monitoring of 97 flip-flops. After a proton fluence of 8.3×10^{12} cm^{-2} (about 10% above the radiation-tolerance criteria) no SEE was detected and the power-on-reset time was stable.

5.4 Controller board

Fast and time critical information (clock, trigger, resets, etc.) are sent from 100 meters away using the Timing, Trigger, and Control distribution system [47]. This system is responsible for the synchronization of the front-end electronics and for the delivery of the correctly phased clock, beam-crossing identification, and trigger-accept signals to all the crates. These signals are fanned out using optical links. A controller board receives the signals and forwards them electrically to the other boards in the crate. This reduces the number of TTC (and SPAC) links that must be provided to the detector. A standard detector-wide mixed analog and digital radiation-tolerant ASIC receiver (TTCrx) on each front-end board decodes the information [47].

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The aim of the serial communication system is to load and read all the registers and memories in the calorimeter electronics. The master of the link resides in the off-detector readout crate and sends the information on a bi-directional optical link to the controller board which fans it out to a slave ASIC on every board in the crate. A slave communicates with the other ASICs on the board using a parallel interface or the I2C protocol. The slave was prototyped in an FPGA and fabricated in DMILL.

The ASIC logic was specifically designed to be resistant to SEE; the critical flip-flops were triplicated and manually placed such that they were not aligned along a common line, and the immunity of the routed design to SEE was thoroughly simulated in hardware description language. Special care was taken to avoid any deadlock situations induced by SEE. The SPAC slave was exposed at PSI, using a 70 MeV proton beam with a flux of $5 \times 10^8\,\mathrm{cm^{-2}s^{-1}}$. Twelve chips were exposed while being monitored online to a fluence of up to $1.1 \times 10^{13}\,\mathrm{cm^{-2}}$ each. No SEE was observed during exposure and all the chips remained functional.

Apart from the radiation-tolerant TTCrx and SPAC slave ASICs, the controller board hosts several types of radiation-tolerant COTS also used on other boards of the front-end electronics, such as the OTx optical transmitters, MC10H116D ECL line receivers, TRR-1B43 optical receivers, and LHC4913 voltage regulators. These components were qualified as part of the qualification process of the other boards.

6. Electronics inside the cryostats

6.1 Cold preamplifier

Preamplifiers immersed in the liquid argon are used to read out the hadronic end-cap calorimeter and are located at a radius of about two meters from the accelerator beam line. In this case, the preamplifier hybrids on the front-end boards are replaced by pre-shaper circuits, which adapt the cold preamplifier output signal to the input of the regular shaping amplifiers (see section 5.1.2).

The cold preamplifiers have been developed in GaAs technology. Eight preamplifiers and two drivers are integrated into each GaAs chip. The outputs of four preamplifiers are fed into the driver input. At the location of the cold electronics in the hadronic end-cap calorimeters of the ATLAS experiment a total ionizing dose of 300 Gy and a neutron fluence of $2 \times 10^{13}\,\mathrm{cm^{-2}s^{-1}}$ (1-MeV neutron equivalent in Si) is expected after 10 years of LHC operation at maximum luminosity.

A series of radiation tests of the final design (GaAs TriQuint QED-A 1 μm technology) of the amplifiers were carried out at the IBR-2 reactor using a high neutron fluence and gamma dose [61]. A set of seven GaAs chip were exposed to neutrons. The preamplifiers were exposed to a total fluence of fast neutrons of $(1.1 \pm 0.2) \times 10^{15}\,\mathrm{cm^{-2}}$ and accompanying gamma dose of (3.5 ± 0.3) kGy. Motherboards with the GaAs chips were kept in a cryostat filled with liquid nitrogen during the whole period of exposure and measurements. Separate tests showed that the performance was the same whether the power was switched on or off during the exposures, so it was switched off in between measurements. The gamma exposure of eight chips was carried out at cold conditions as well. A total ionizing dose of (55 ± 8) kGy was collected with an accompanying fast neutron fluence of $(1.1 \pm 0.2) \times 10^{14}\,\mathrm{cm^{-2}}$. The chips performed well to radiation exposures more than 25 times the radiation-tolerance criterion. In general, the results are in agreement with the

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previous tests of the prototypes and measurements performed at different radiation facilities and institutes [62].

The preamplifiers showed a stable performance in terms of transfer function, peaking time, and linearity up to a neutron fluence of 5×10^{14} cm^{-2}, independent of the detector capacitance. For neutron fluences beyond this value, a clear deterioration of the transfer function and linearity has been observed. Under gamma exposure no deterioration in performance has been seen up to a total ionizing dose of 55 kGy.

The equivalent noise current increases under exposure to neutrons and photons. The noise increase is more significant under photon exposure. It has been found that the noise increase under neutron and photon exposure was due to an increase of the parallel noise, while the series noise remains almost constant up to the highest radiation dose.

6.2 Cables and connectors

Custom designed micro-coaxial cables with connectors were used in the liquid argon [63]. These cables had to satisfy very stringent requirements in terms of signal transmission, dimensions, and radiation tolerance. The cables and connectors were manufactured with materials known to be radiation tolerant. To be certain, they were tested for possible deterioration under photon and neutron exposures in air and in liquid argon. A ^{60}Co source at Pagure was used to deliver 80 kGy of total ionizing dose. No damage was observed. Measurements after exposure were found to be compatible within the measurement errors to those before the exposure. The IBR-2 was used to obtain a neutron fluence of 1.8×10^{16} cm^{-2}. The difference in cable capacitance after neutron exposure was small, and within the measurement errors and changes due to humidity. These tests were performed on cables in air. A second set of cables were exposed in liquid argon. No significant change in the argon pollution was measured to a total fluence of 7.0×10^{15} cm^{-2} and dose of about 70 kGy. These radiation levels are high enough to cover the wide range of doses anticipated in the calorimeter at high luminosity.

7. Summary

We have designed, developed, and built a mixed analog and digital processing system to read out the 190 000 channels of the ATLAS liquid argon calorimeters. Table 9 shows the maximum radiation levels to which each component was tested. The system has been radiation qualified to withstand ionizing radiation levels of 10 Gy/yr, non-ionizing energy loss effects from neutrons at a flux 3×10^{11} cm^{-2}yr^{-1} (1-MeV neutron equivalent in Si), and single-event events from hadrons at a flux of 6×10^{3} cm^{-2}s^{-1}, for a period of 10 years of LHC operation. To achieve this level of radiation tolerance, a combination of ASICs designed in radiation-tolerant technologies and radiation-tolerant COTS have been tested using ^{60}Co gamma-ray sources and X-rays, as well as neutrons and protons to radiation levels often in excess of 70 times those anticipated within ATLAS. Each component in the electronic system had to satisfy a set of radiation-tolerance criterion to be pre-selected and qualified for use within ATLAS. All the resulting components selected for use in ATLAS have met the radiation-tolerance requirements.

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Table 9. Maximum radiation levels to which each component was tested. A * behind a number means that the value was derived from the radiation levels of a different type of radiation (usually protons). The components are ordered according to semiconductor technology.

Component	TID (kGy)	Neutron (10^{13} cm^{-2})	Proton (10^{13} cm^{-2})
Warm preamp	1.8*	11	
Pre-shaper	1.2*	27	
Cold preamp	55*	110	
Shaper	2.0	1.7	
Op-amp	2.0	9.0	
HAMAC	3.0	4.5	
SPAC slave		1.1	
CONFIG	12*	1.3*	1.8
SMUX	15	30	0.12
BIMUX	3.5	3.2	3.0
DAC	2.0	9.2	
CALOGIC			0.83
GSEL	16*	1.8*	2.4
SCAC	44	1.9	4.9
CLKFO	17*	1.8*	2.5
QPLL	17*	1.8*	2.5
LHC7913	17*	1.8*	2.5
HFA1135	8.7	3.2	3.0
MC10H116	18*	2.1*	2.8
AD9042	10	2.0	
AD8042	27*	2.9*	3.9
AD8011	3.5	3.2	3.0
AD8001	3.5	3.2	3.0
HDMP-1022	43	48	2.8
OTx	43	48	2.8
Optical fiber	2.8	2.0	
Cold cable	80	1800	

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