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ATLAS liquid argon calorimeter front end electronics

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ABSTRACT: The ATLAS detector has been designed for operation at CERN's Large Hadron Collider. ATLAS includes a complex system of liquid argon calorimeters. This paper describes the architecture and implementation of the system of custom front end electronics developed for the readout of the ATLAS liquid argon calorimeters.

KEYWORDS: Electronic detector readout concepts (gas, liquid); Calorimeters; Front-end electronics for detector readout.

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1. Introduction

ATLAS [1] is a large general-purpose detector designed for operation at the Large Hadron Collider (LHC) at CERN. The LHC is a proton-proton collider which will operate with a center-of-mass energy of 14 TeV. A system of liquid argon (LAr) calorimeters forms one of the major ATLAS detector systems. The LAr calorimeter system is composed of an electromagnetic (EM) calorimeter covering the region of pseudorapidity $|\eta| < 3.2$, a hadronic endcap (HEC) calorimeter covering $1.5 < |\eta| < 3.2$, and a forward calorimeter (FCAL) covering $3.1 < |\eta| < 4.9$. These elements are housed in three cryostats. The central (barrel) cryostat contains the barrel EM calorimeter (EMB), which covers $|\eta| < 1.5$. There are two endcap (EC) cryostats, each containing one side of the endcap EM calorimeter (EMEC), the HEC and the FCAL. Each element of the LAr calorimeter system is segmented in depth: the EMB and EMEC each have four layers (presampler, strips, middle and back), the HEC has three layers, and the FCAL also has three (one electromagnetic layer and two hadronic layers). More details about the design, construction, and performance of the calorimeters themselves can be found in reference [2].

As depicted schematically in figure 1, the electronic readout of the ATLAS LAr calorimeters is divided into a Front End (FE) system of boards mounted in custom crates directly on the cryostat feedthroughs, and a Back End (BE) system of VME-based boards located in an off-detector underground counting house (dubbed USA15) where there is no radiation. The design and implementation of the BE system, which includes Digital Signal Processor (DSP) electronics for digital filtering of the readout signals in order to reconstruct the deposited energy and other quantities, are described in reference [3]. The purpose of this note is to describe the overall architecture and implementation of the ATLAS LAr FE system. A subsequent publication will describe the measured system performance of the overall ATLAS LAr readout.

This paper is organized as follows: An overview of the LAr FE electronics system is presented in the next section. Then the various custom boards designed for implementing the readout and the Level 1 (L1) trigger are described in sections 3 and 4, respectively. This is followed in section 5 by a description of the FE infrastructure. Sections 6 and 7 then describe the low voltage power supply (LVPS) and high voltage power supply (HVPS) systems, respectively, followed in sections 8 and 9 by discussions of the grounding scheme and cable plant. Finally, a summary is presented in section 10.

2. Overview of ATLAS LAr Front End electronics

Given the fine segmentation of the ATLAS LAr calorimeters, a total of 182468 active channels must be read out. The FE electronics faces demanding requirements [4], which include the following:

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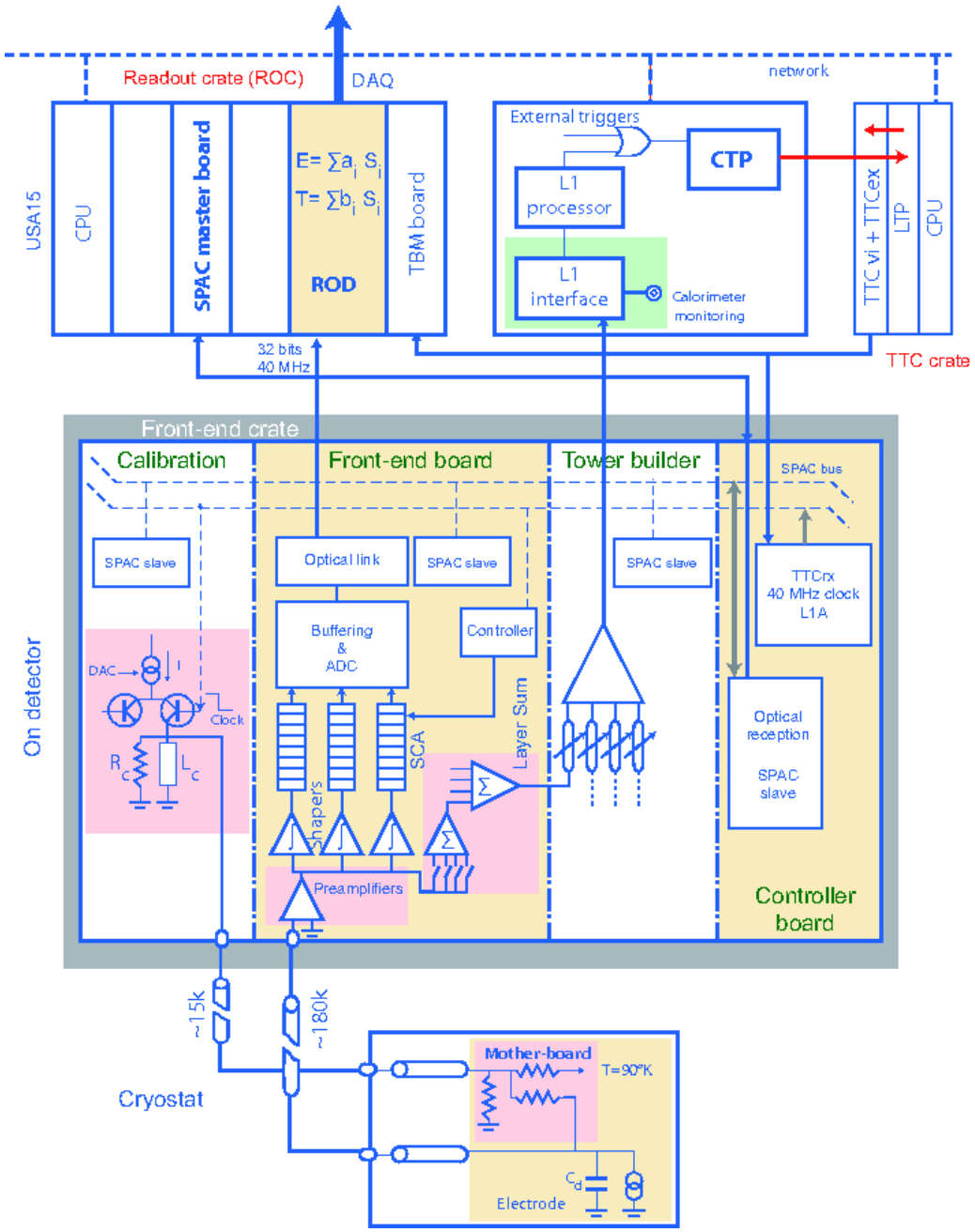

Figure 1. Block diagram depicting the architecture of the overall ATLAS LAr readout electronics. The lower box depicts the calorimeters installed in their respective cryostats. The central box illustrates the functionality of the FE boards located in FE crates mounted on the cryostat feedthroughs. The upper layer shows the off-detector BE electronics mounted in Readout Crates, as well as trigger and TTC (control) crates.

- the calorimeter signals must be sampled at the LHC bunch crossing frequency of 40 MHz. The signals must be stored during the latency of the L1 trigger of up to 2.5 μs (100 bunch crossings). For triggered events, the readout must be accomplished without significant dead-time for a maximum mean L1 trigger rate of 75 kHz.

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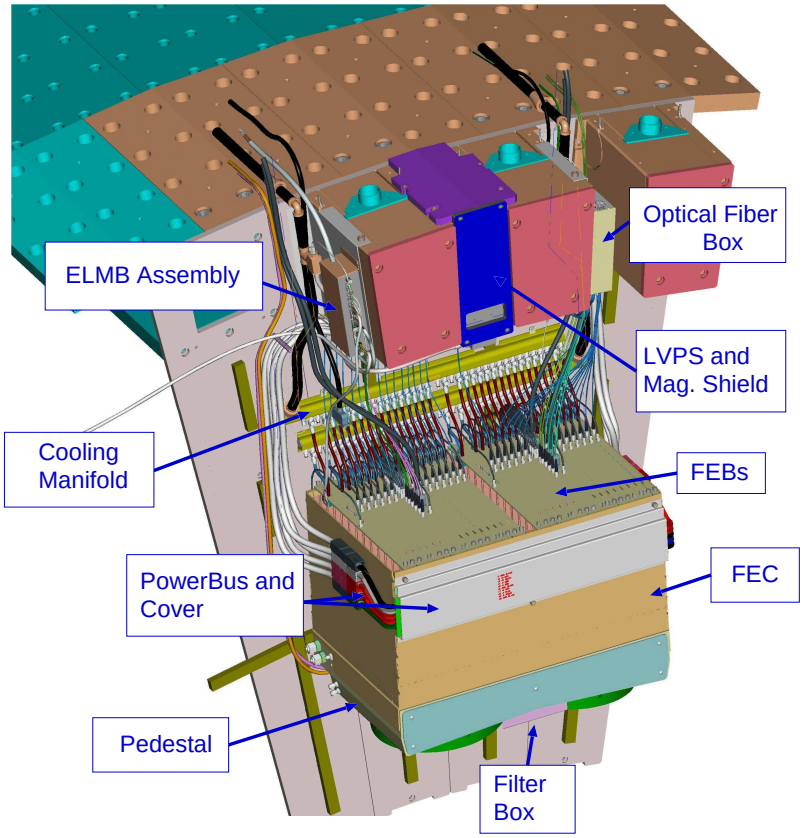

Figure 2. Diagram depicting the arrangement of LAr FE components, services, and infrastructure in the vicinity of one FEC.

- the energy deposited in each calorimeter cell must be measured with a precision of better than 0.25% at high energy. A dynamic range of ≈ 17 bits is needed to cover the energy range of interest, from a lower limit of ≈ 10 MeV set by the noise levels up to a maximum of 3 TeV. The coherent noise over many cells must be maintained below 5% of the total noise per channel.

- the time of the energy deposition in each calorimeter cell must be measured with a precision of ≈ 100 ps for high energy pulses.

- analog sums corresponding to L1 trigger towers of size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ must be delivered for use by the L1 trigger system.

Given the stringent noise requirements, the LAr FE electronics boards are placed in crates mounted directly on the calorimeter cryostat feedthroughs, around the circumference of the calorimeter. Figure 2 shows the arrangement of the major components of the system in the vicinity of one Front End Crate (FEC).

Figure 3 shows a photograph of one end of the EMB cryostat, in which a number of the FECs are visible. The spaces between FECs are heavily used for the routing of cables and other services to the ATLAS inner tracking detectors, so strict attention must be paid to staying within

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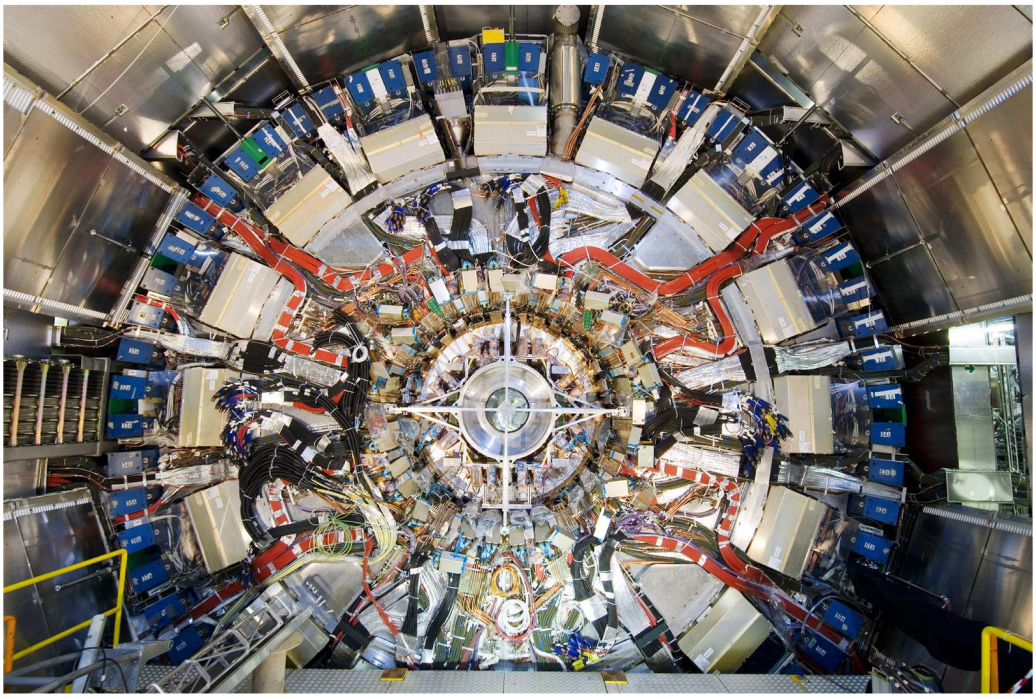

Figure 3. Photograph of one end of the EMB cryostat, taken in June 2007 during installation and integration of the inner tracker endcap. The LAr FECs are visible around the circumference of the cryostat.

the envelope of space assigned for the LAr electronics. This on-detector location demands many additional requirements, including tolerance of significant levels of radiation. Achieving a high channel density and low power is important. The FE boards must be cooled to remove any heat dissipated. Access is very limited, so reliability is a key concern.

The radiation tolerance issues required that all electronics components selected for use on the detector be subjected to an extensive radiation qualification process [5]. This led to the development of a number of custom Application Specific Integrated Circuits (ASICs) in specialized, radiation-tolerant semiconductor processes, and to a very limited use of commercial components. A number of ASICs were developed in the DMILL process [6], and several more using a commercial 0.25 μm "deep submicron" (DSM) process, but using a special library which was radiation hardened through the use of a custom-developed enclosed transistor geometry [7]. Details of the radiation qualification procedures and results will be outlined in a subsequent publication.

As was shown in figure 1, the FE system includes Front End Boards (FEB), which perform the amplification, shaping, sampling, storage, digitization, and readout of the calorimeter signals. Calibration (CALIB) boards inject precision calibration signals, and Tower Builder Boards (TBB) and Tower Driver Boards (TDB) produce analog sums for the L1 trigger. The various boards in the FECs require control signals for proper operation. These signals include the 40 MHz LHC clock, the L1 Accept signal from the trigger, and other fast synchronous signals provided as part of the ATLAS Trigger, Timing and Control (TTC) system [8]. In addition, most of the boards need to be configured and monitored by writing or reading back the values of various on-board registers and other resources. A custom serial link known as SPAC (Serial Protocol for the ATLAS

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Table 1. Summary of the numbers of the various main FE boards for the different LAr calorimeters.

HFEC Type	HFEC	FEB	CALIB	CONT	TBB	TDB
EMB	64	896	64	64	64	-
EMEC Std	32	416	32	32	32	-
EMEC Special	8	136	16	16	24	-
HEC	8	48	8	8	-	16
FCAL	2	28	2	2	-	4
Total	114	1524	122	122	120	20

Calorimeters) [9] is used for this purpose. Controller (CONT) boards installed in the FECs are used to receive and distribute the TTC and SPAC signals to the various FE boards.

Each FEC is divided mechanically into two halves. The bus that distributes power to the boards traverses the entire crate, but for most other purposes the basic element of the FE electronics is one Half FEC (HFEC). The configuration of each HFEC depends on the calorimeter to which it is connected. The EMB is equipped with 32 FE crates, configured as 64 identical EMB HFECs. The readout of the EMEC includes 16 dedicated EMEC crates, configured to provide 32 "EMEC Standard" HFECs. In addition, a set of eight crates are shared between the EMEC and the HEC, providing eight "EMEC Special" HFECs and eight HEC HFECs. The FCAL has two dedicated crates, which are only half-equipped in order to provide the necesary two FCAL HFECs. Table 1 summarizes the numbers of the various types of FE boards in each type of HFEC. Note that a total of 1524 FEBs is required to read out the entire calorimeter system.

3. Front End electronics boards

The custom FE boards must meet the mechanical constraints of the FEC. The external dimensions of the boards must be 490 mm $\times$ 409.5 mm, and the board thickness is limited to a maximum of 2.54 mm. Figure 4 illustrates the required board dimensions, and all the connectors and their locations. Connectors are mounted along three edges of the boards. Connectors along the front panel side bring in the TTC signal and provide outputs to the BE electronics. On the opposite edge, connections to the FEC baseplane are made. Finally, the power and SPAC connections are made along one side edge of the boards. Boards are located in the FEC with a pitch of 800 mils (20.3 mm). However, unlike the case for VME-style boards, the boards are mounted in the center relative to their front panel.

3.1 Front End board

The FE readout of the LAr calorimeters is implemented on the 128-channel FEB. A detailed description of the design and implementation of the FEB can be found in reference [4]. Here we describe only a few of the most salient details.

A block diagram indicating the main features of one four-channel element of the FEB architecture is shown in figure 5. The raw signals from the calorimeter are mapped onto the FEB inputs

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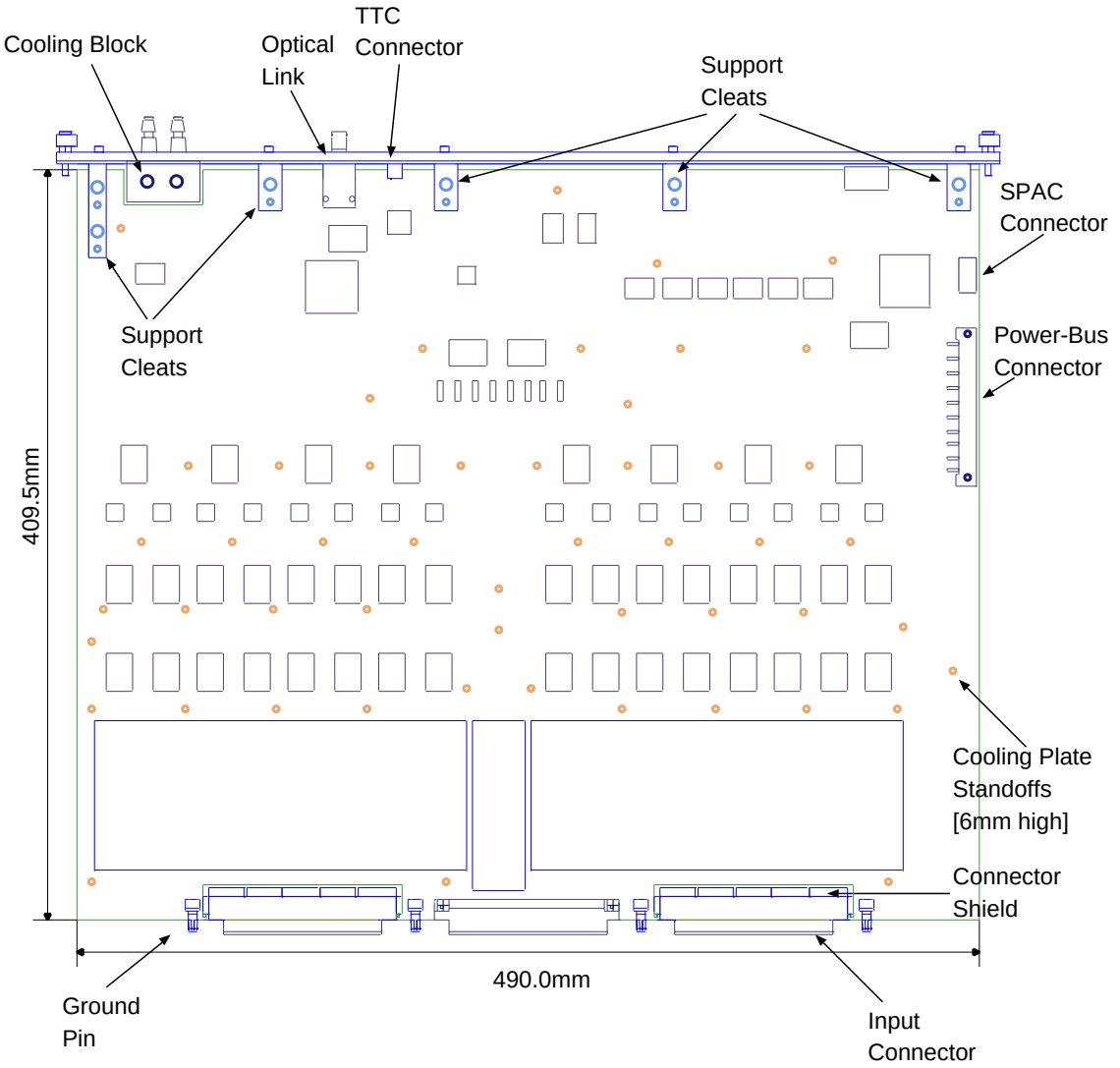

Figure 4. Mechanical drawing of the FE electronics boards showing board dimensions, connector locations, and locations of the front panel supports.

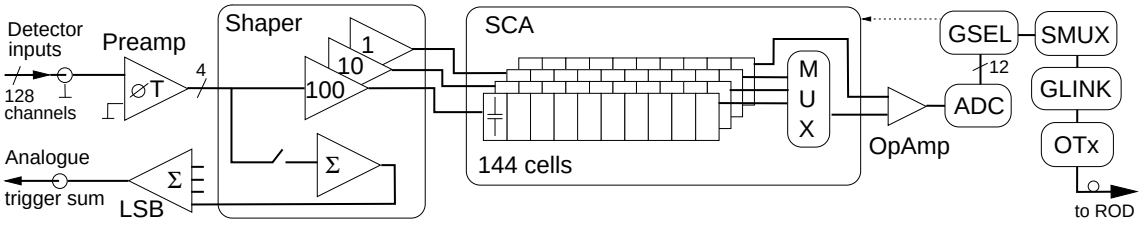

Figure 5. Block diagram of the FEB architecture, depicting the data flow for four of the 128 readout channels per FEB.

as they emerge from the cryostat feedthroughs. On the FEB, the signals are first subject to several stages of analog processing. Preamplifier hybrids amplify the raw signals, which are then split and

further amplified by shaper chips to produce three overlapping linear gain scales, with gain ratios of ≈ 10. Each signal is subject to a fast bipolar CR-$(RC)^2$ shaping function with τ = RC = 13 ns. The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz by switched-capacitor array (SCA) analog pipeline chips, which store the signals in analog form during the L1 trigger latency.

For events accepted by the L1 trigger, typically five samples per channel are read out from the SCA using the optimal gain scale, and digitized using a 12-bit Analog-to-Digital Converter (ADC). The digitized data are formatted, multiplexed, serialized, and then transmitted optically out of the detector to the Readout Driver (ROD) in USA15 via a single 1.6 Gbps optical output link per FEB.

In addition to reading out the individual calorimeter channels, the FEB performs the first two stages of summing in preparation of analog sums used by the L1 trigger system. Each shaper chip outputs a sum of its four input channels. These partial sums are routed to two Layer Sum Boards (LSBs) on each FEB that perform further summing, depending on the region of the calorimeter to which the board is connected, and then drive the sums through the FEC baseplane to the corresponding TBB or TDB in that HFEC.

The performance of the FEBs meets or exceeds the specifications of the LAr readout. The dynamic range is ≈ 17 bits. The low end of the range, corresponding to a few MeV, keeps the FEB contribution to the noise below the level of the calorimeter and preamplifier noise. The high end of the range corresponds to $\approx$3 TeV, the highest energy one might expect to be deposited at the LHC in a single channel of the ATLAS EM calorimeters. Amplitude and timing resolutions for large pulses are better than 0.1% and $\approx$20 ps respectively. The typical coherent noise per channel is $\approx$2-3% of the total noise.

3.2 Calibration board

The electronic calibration of the LAr readout is performed by injecting precision pulses into the cryostat from a CALIB board mounted in the FEC. A detailed description of the design and implementation of the CALIB can be found in reference [10]. Here we briefly describe only a few of the main features.

A uniform, stable and linear signal whose shape is close to the triangular ionization signal of the calorimeter is provided to all channels. A schematic diagram of this calibration system is displayed in figure 6. A voltage pulse, propagated inside the calorimeter with a cable of impedance R_0, is applied across a 0.1% accuracy injection resistor (R_{Inj}) mounted inside the cryostat on the detector. This pulse is distributed to groups of nearby channels with little or no crosstalk in the detector.

The CALIB houses 128 identical channels. A precise current (I_p) is built from a custom Digital-to-Analog Converter (DAC) ASIC with 16-bit dynamic range, the design of which is based on an R/2R architecture. This DAC shows a stability (with time and temperature) better than 0.1% and an integral nonlinearity better than 0.1%. A custom low-offset operational amplifier (Opamp) is used to distribute the DAC to the 128 channels with minimal voltage drop. Fuses are used to trim the offset to the desired accuracy ($< 50\ \mu$V). The voltage pulse is converted to current using an external 0.1% resistor. A star configuration has been implemented to distribute uniformly this voltage to all channels on the CALIB, necessitating special care during the printed circuit board (PCB) design. A high frequency switch made of a PMOS/NPN pair turns off the current when a

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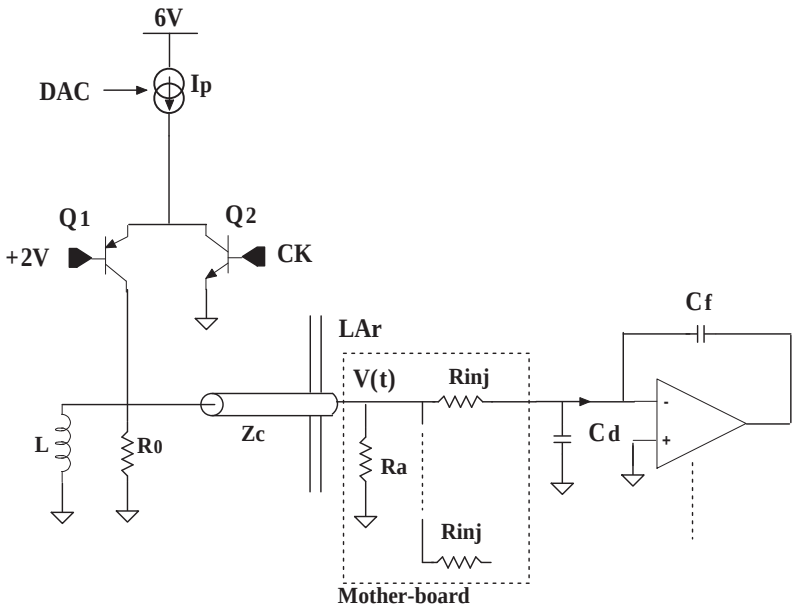

Figure 6. Schematic diagram of the calibration scheme for the EM calorimeters. For more details, see the text.

command pulse is applied. The magnetic energy stored in the inductor is transferred to the resistor R_0 and output cable, producing a fast voltage pulse with an exponential decay.

Communication of the CALIB with the external world is done through the SPAC and TTC systems. Control of the CALIB and the loading of the parameters, including channel enable and DAC value, uses a custom digital ASIC dubbed CALOGIC.

The overall CALIB performance fulfills the ATLAS specifications. All integral nonlinearities are better than 0.1% and the channel-to-channel uniformity is better than 0.2%.

3.3 Controller board

The function of the Controller is to receive the TTC and SPAC control signals from USA15 and to fan them out and deliver them to the various FE boards in the same HFEC. Providing a local fanout in the FEC greatly reduces the number of long TTC and SPAC links that must be provided from USA15 to the detector. As was shown in table 1, each EMEC Special HFEC holds two Controllers, while all other HFECs hold one. A total of 122 Controllers are needed for the entire LAr system.

A functional diagram of the Controller, as well as a photograph, are shown in figure 7. The Controller receives optically from USA15 the TTC and SPAC signals, and converts them to electrical signals. The timing-sensitive TTC signals are distributed to each FE board using point-to-point connections, while the slower SPAC signals are fanned out via a dedicated SPAC bus mounted along the side of the crate.

Table 2 provides the specifications of the different TTC signals and the SPAC bus implemented for each FEC type. Dmax is the maximum distance (in number of slots as well as in mm) between the Controller and any of the boards to which it has to provide the TTC signal.

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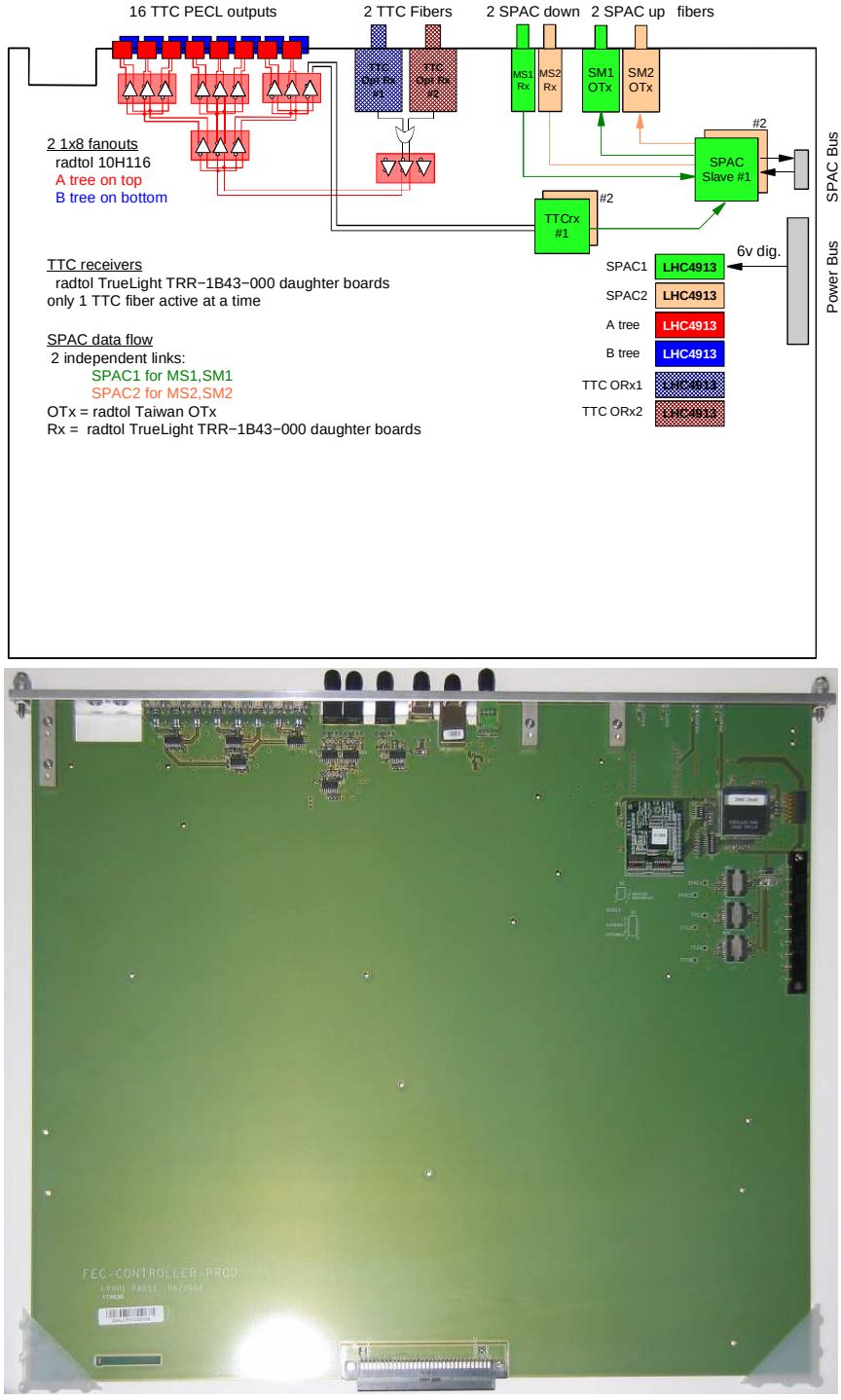

Figure 7. Functional diagram (upper) and photograph (lower) of the Controller. The optical connectors are visible near the center of the front panel at the top of the photograph, to the left of which are the chips fanning out the TTC signal. The SPAC slave and voltage regulators are mounted near the SPAC and power connectors on the right. The connector at the bottom connects to the FEC baseplane to provide alignment and mechanical support to the Controller, but does not have any signals connected.

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Table 2. Summary of the TTC links and SPAC bus configurations in the various FE crates.

HFEC Type	Number of Boards in Fanout	SPAC Bus Length (slots)	Dmax	
			(slots)	(mm)
Barrel	16	19	9	183
EMEC Standard	15	19	9	183
EMEC Special 1	11	12	9	183
EMEC Special 2	11	12	11	223
HEC	7	12	9	183
FCAL	15	19	11	223

Trigger, Timing and Control distribution

The TTC signals are driven optically from the TTC crate located in USA15 and received at each Controller by optical receivers mounted on its front panel. To enhance reliability, the Controller is equipped with two TTC optical receivers, each connected to an individual optical fiber. To reduce the logic on the Controller, and thereby enhance the system reliability, no specific choice is made on the Controller to decide which of the two incoming TTC signals to use. Instead, this choice is made in USA15, an accessible area, by connecting the desired optical fiber to the TTC optical output.

The TTC signal is distributed through a tree of commercial driver chips, configured in positive emitter-coupled logic (PECL) format, with 18 terminations. Two of the signals are used on the Controller by the two TTC Receiver (TTCRx) chips to handle independently the Controller's two on-board SPAC slaves. For reliability purposes, this distribution tree is organised as two independent branches. In case of problems with one of the branches, at most half of the TTC signals are lost.

The PECL TTC signals are output through 16 Universal Serial Bus (USB) "mini-B" surface-mount component (SMC) connectors on the Controller front panel. Custom one-meter halogen-free USB mini-B/mini-B cables deliver the TTC signal from the Controller to the other boards of the FEC. The differential impedance of the cable was measured to be $\approx 90\Omega$. Due to the tight space requirements, the 16 mini-B connectors are placed on both sides of the Controller PCB, eight on the top and eight on the bottom. To ease plugging in the cables, the connectors are mounted on SMC-like custom daughterboards.

SPAC serial control system and distribution

The general layout of the SPAC serial communication system is shown in figure 8. This link is used to load, update, or read back the various registers and memories of the FE boards through VME commands sent to the SPAC Master boards [11], located in the ROD crates in USA15. Each serial network consists of one Master and multiple Slaves.

The SPAC protocol, described in more detail in appendix A, requires at least two unidirectional lines: one Master-to-Slave line (MS) and one Slave-to-Master line (SM). These are transmitted on separate unidirectional optical links between SPAC Masters in USA15 and Controllers in FECs mounted on the detector. For reliability purposes, the downstream and upstream serial lines are both duplicated (upstream lines: SM1, SM2; downstream lines: MS1, MS2). At any time, only

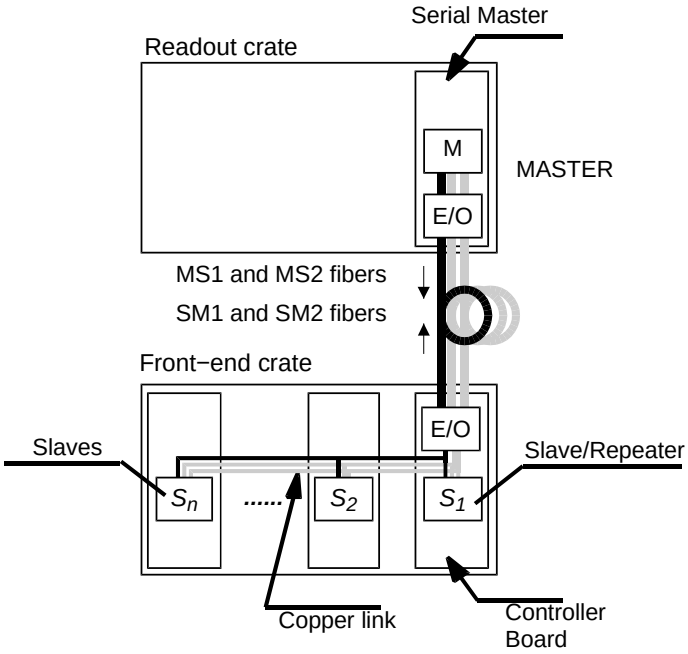

Figure 8. Architecture of the SPAC serial control system.

one of the two downstream lines carries the useful information, the other line remaining idle (the decision is made on the Master in USA15). Each Slave receives both lines and automatically detects which is active and which is idle. The upstream serial lines SM1 and SM2, on the other hand, both carry the same information at the same time. This scheme limits the decision logic on the remote Slave side and therefore improves the reliability of the system.

The optical signals are converted into electrical differential signals on the Controller and transferred on a copper bus to the various FE boards housing the Slaves. To improve the reliability and the noise immunity of the system, the serial bus is implemented in a differential technology. While the Master boards, sitting in the radiation-free environment of USA15, consist of programmable logical devices housed on VME boards, the Slaves are located in the FE crates, and therefore their functionality is implemented in a custom radiation-tolerant ASIC.

A functional diagram of the SPAC Slave ASIC is shown in figure 9 and a detailed description of the chip is given in reference [9]. The Slave receives the incoming frames from the Master on the MS serial inputs, decodes the different fields of the frames and, if required, communicates with its host board. Finally, the Slave encodes its reply frame and sends it back to the Master via the SM serial outputs.

The Slave provides to the board on which it is mounted a parallel interface to read and write, under request of the Master, the various on-board registers or other resources. These resources are identified with a 7-bit subaddress, and can be 8-, 16- or 32-bit registers, or a block of memory bytes of arbitrary length. Several subaddresses are reserved to access some internal resources of the Slave. The Slave also provides to the board an Inter-integrated circuit (I2C) master interface. I2C interfaced components on the board can therefore be controlled through read or write accesses to some dedicated internal registers of the Slave.

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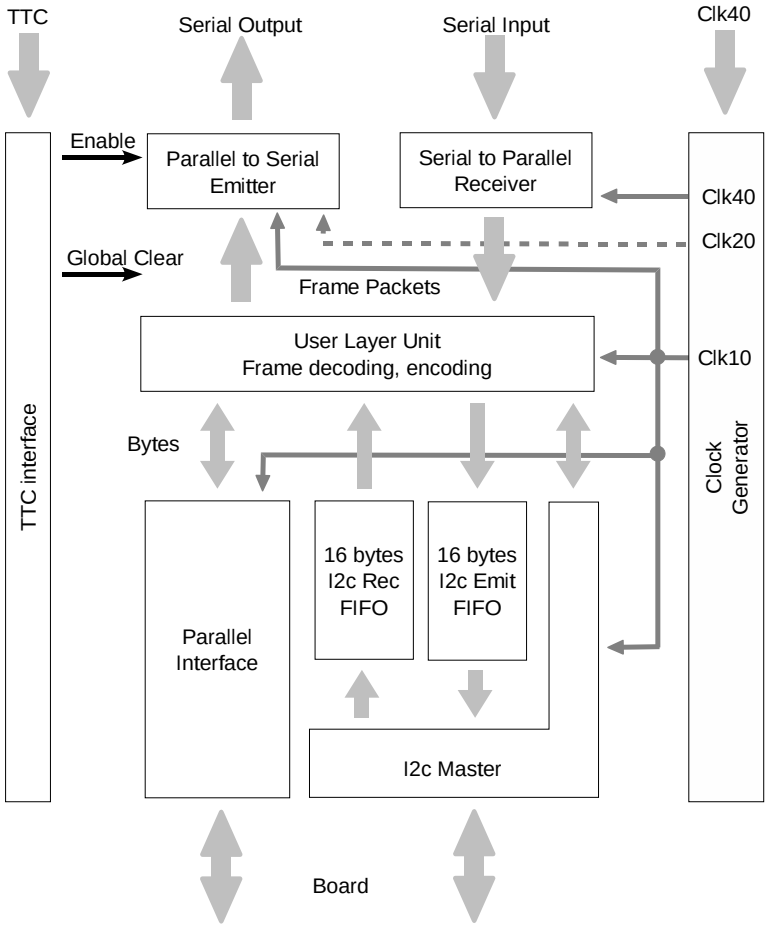

Figure 9. Functional block diagram of the SPAC slave ASIC.

Typically, the Slave ASIC communicates through its I2C interface with the CALOGIC ASIC on the CALIB, through the parallel interface with the Configuration Controller on the FEB, and with the Bimux chips on the TBB. On each board, the Slave ASIC receives its clock from the on-board TTCrx chip.

The SPAC slaves on the Controller are set in a repeater mode, which is a different configuration than the SPAC slaves of the other FE boards. In this mode, they repeat the MS signal that is optically received by the Controller to one of the two MS lines of the SPAC bus. They also transmit the SM signal from the SPAC bus line to the optical tranceivers that send this signal to the SPAC Master. Both SPAC Slaves receive MS1 and MS2 signals, but drive only one MS signal each on the SPAC bus and return only one SM line back to the Master.

It was decided to use optical components on the Controller that had been radiation qualified for other uses in ATLAS, after validating that the components were also appropriate for the optical transmission of SPAC signals. The custom 850 nm optical transmitter used to transmit the output data from the the FEB to the BE electronics is used for transmitting the SM data from the Controller to USA15. It was tested to verify its performance for the relatively slow SPAC signals. The MS

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fibers are received on the Controller using a commercial 1300 nm optical receiver which is also used for receiving the TTC signals. As a result of these choices, note that the optical wavelength of the incoming and outcoming signals are different, so the optical transmitters and receivers on the SPAC Master side in USA15 are of course matched appropriately.

Production and testing of the controller

The Controllers must respect the constraints of the FEC environment. Two major constraints are the presence of cooling plates on each side of the board, limiting the thickness of the components to about 5.5 mm, and the presence of matter partially covering the top of the FEC, limiting the available space on the front panel. As mentioned previously, these constraints required mounting the output TTC connectors on both sides on the PCB.

The TTCrx chips are mounted on daughterboards called TTCrxDCU2 boards which integrate one TTCrx and one I2C-interfaced Detector Control Unit (DCU) [12] chip used to monitor temperatures and voltages. The same daughterboards are used on the TBB. Using daughterboards allowed a reduction in production costs, as the TTCrx ball-grid-array package requires the use of higher class PCBs and assembly techniques. The hardwired addresses of the two TTCrx chips on the board are defined by switches located on the daughterboard. The SPAC Slaves can configure their associated TTCrx via I2C commands.

The Controller PCB is made of eight layers. The most critical lines are routed on impedance-controlled striplines in inner layers between two ground or power planes. For reliability purposes, the different Controller functions are partitioned such that six different power levels are used, routed on two power planes. The power consumption is 1.5 A on the digital 6 V power line.

A total of 135 Controllers have been produced, while 122 are needed for installation in ATLAS. The TTCrxDCU2 daughterboards have been produced and tested as an individual component before plugging onto the Controllers. The SPAC Slave chips were also tested on a separate jig before Controller assembly. The Controller production sequence included standard continuity tests performed after PCB fabrication. The assembly of the components (including the various daughterboards) was done in industry. The boards were then subjected to a standard burn-in procedure together with a subsequent functional test. The quality of the TTC signals on each TTC output was measured and recorded. The SPAC functionality was also checked.

The system performance of the Controller was validated using both tests on a dedicated setup in Paris and system tests performed at Brookhaven National Lab (BNL). At BNL, the final Controller prototype was installed and tested successfully in a system that included a SPAC Master plus 14 FEBs and a CALIB. The test verified that a fully loaded HFEC could be reliably configured. It was also shown that the TTC fanout of the Controller and sending the TTC signal to the FEBs via cables did not degrade in a significant manner the quality of the TTC signal.

An investigation was made of the effect of SPAC activity on the coherent noise measured in the FEBs. The coherent noise was measured and compared in a variety of conditions, including when the SPAC bus was completely quiet due to the Controller being disconnected from the MS fibers (SPAC Off), when the SPAC bus was not isolated from the optical receivers and a carrier is generated on the MS lines (SPAC On), and when SPAC frames are being transmitted on the bus. Having some SPAC activity on the bus increased by typically only 5% the coherent noise on the

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FEBs. In all cases, the coherent noise per channel was always below 3% of the total noise per channel, still meeting the specification to be less than 5%.

Tests of the redundancy of the SPAC and TTC optical links were performed. The TTC signal can be received with either TTCrx, without any difference. The duplicated MS and SM lines were also tested. Communication could also be performed with FEBs even when the Controller did not have a valid clock, and with or without the carrier on the download and readback lines. Various failure modes, and in particular the influence of possible dead FEBs, were also investigated. It was shown that it was possible to communicate reliably even in the most extreme case of only one functional FEB with the other 15 boards connected to the SPAC bus but with their power switched off.

4. Level 1 trigger electronics

The LAr readout electronics must form analog sums proportional to the transverse energy (E_T) deposited in each of the LAr trigger towers, and transmit these sums to the L1 trigger system. In the EMB, a trigger tower is a $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ section of the calorimeter, containing 60 cells distributed among four layers in depth. In the endcaps, the trigger tower size and the number of cells per trigger tower depend on η.

The analog sums are made through a multi-stage analog summing tree. The first two stages are implemented in the FEB, where each shaper chip provides a sum of its four input channels, and these four-channel sums are then further summed in the LSBs plugged on to the FEB (more details are provided in reference [4]). The LSB output sums are driven over the FEC baseplane to a dedicated trigger slot. Into that slot is installed a TBB (for the EMB and EMEC) or TDB (for the HEC and FCAL). The TBB/TDB drive their analog sum outputs over long copper cables to USA15, where they are received by the L1 Trigger Receiver/Monitor System. The Receiver provides the final analog sums to the L1 calorimeter trigger (L1CAL) system, where they are digitized at 40 MHz and then digitally processed in the L1 trigger logic.

The LAr trigger electronics, namely TBB, TDB, and Receiver/Monitor are described in more detail in the following subsections. Details of the ATLAS L1 trigger system can be found in reference [13].

4.1 Tower Builder Board

The Tower Builder Board (TBB) is a key element of the L1 trigger chain for the EM calorimeters. The TBB receives via the FEC baseplane the LSB output sums from each of the FEBs. The cabling of the EM detectors is such that one FEB receives signals from a single depth layer (presampler, front, middle, back) of the EM calorimeter. The TBB adds the four signals coming from each layer to form the sum for the complete trigger tower. Each TBB handles the signals for 32 separate trigger towers, and then drives the resulting output signals over two 70 m 16-twisted-pair cables to the Receiver in USA15.

The output sums of the TBB must be proportional to E_T, independent of the sharing of the energy among the layers, with a gain such that an output amplitude of 2.5 V corresponds to 256 GeV. The precision of this gain should be better than 5%, and the integral nonlinearity over this range must be better than 1%. The noise of the total trigger chain is expected to be $\approx$500 MeV (E_T) per

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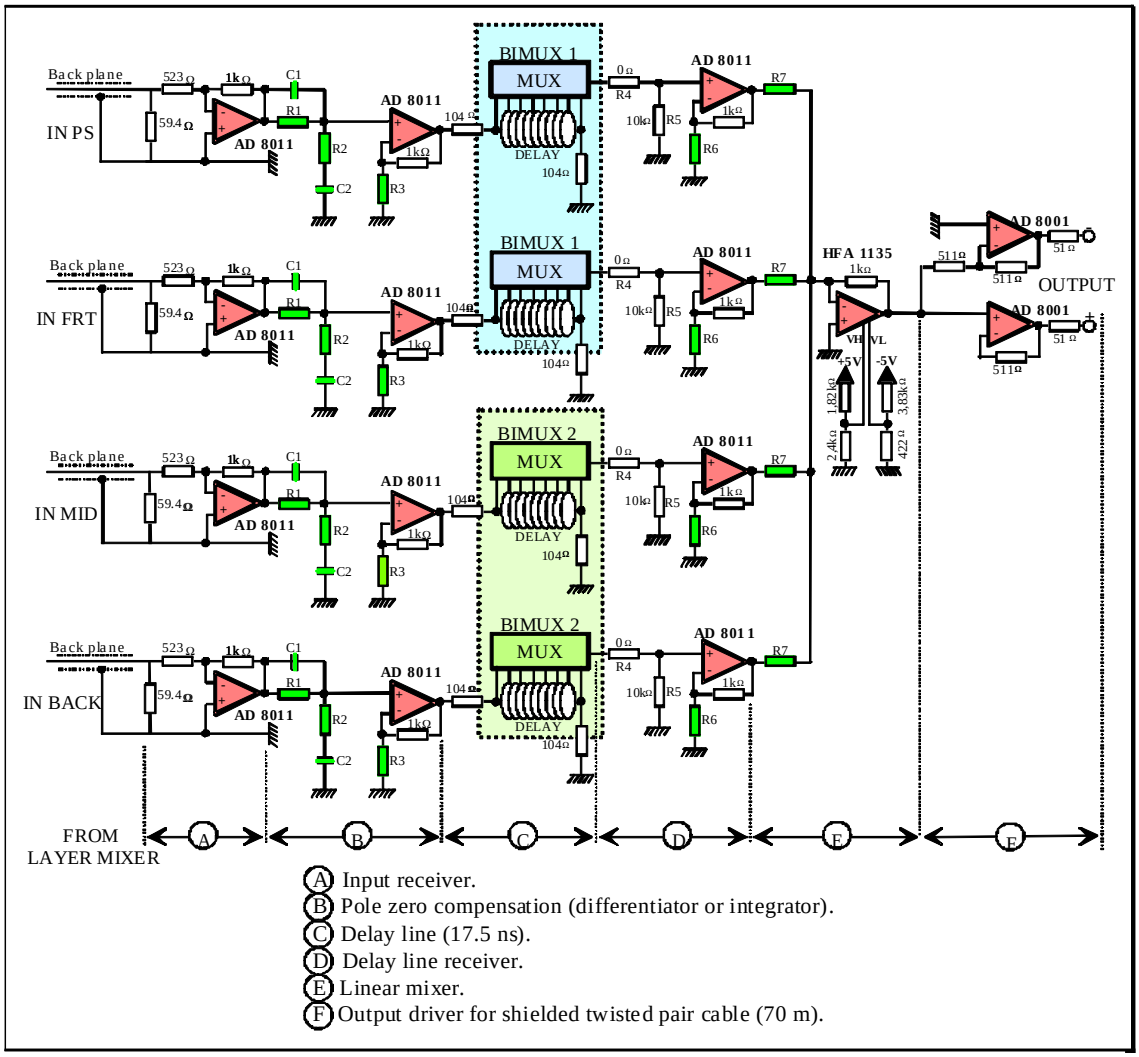

Figure 10. Schematic diagram of one of the 32 analog summation circuits of the TBB. See the text for more details.

trigger tower at η = 0, and the TBB contribution should be negligible. The TBB output signal should have a peaking time of 35 ns, within a few ns.

The trigger chain is designed to deliver a signal rising linearly with E_T up to 2.5 V at 256 GeV. Saturation of the trigger chain is a normal working mode of the trigger. For energies above 256 GeV, the signal should not decrease below 2.5 V, since otherwise trigger errors could result. This implies clamping at all gain and summation stages to avoid deformation of the falling edge of the trigger pulse.

Before summing the four signals of one tower, the TBB must adjust the shapes, gains and delays of its input signals so that they match. As shown in figure 10, each summation circuit is made of six stages (labelled A to F):

(A) the input receiver (50 Ω termination; gain = -2),

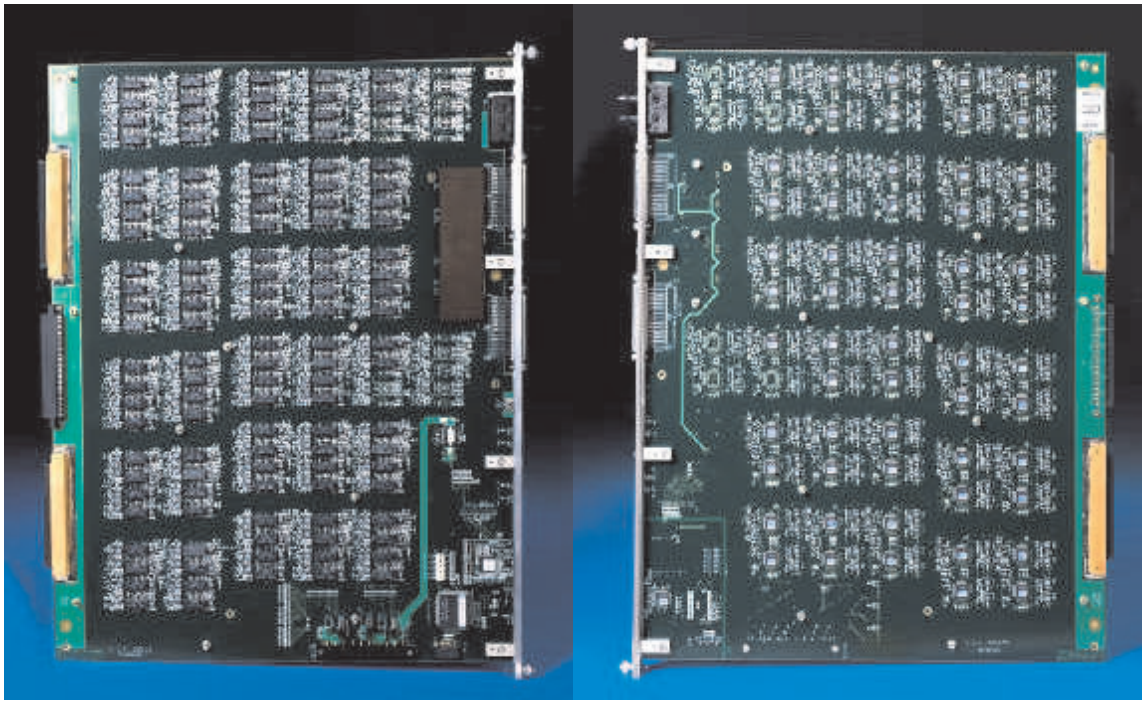

Figure 11. Photographs of both sides of the TBB. The active components are grouped according to the 32 analog summation cells of four channels each.

(B) the pole zero compensation (it adjusts the signal peaking time by integration or differentiation depending if C1 or C2 are removed/short-circuited or not, and compensates the resulting amplitude modification by gain; the magnitude of these corrections is adjusted for each channel by varying the values of R1, R2 and R3),

(C) the delay line (it compensates the differences in cable lengths and values of particle flight time between the four inputs; an analog multiplexer (the Bimux) under software control allows to choose among 8 delay values from 0 to 17.5 ns),

(D) the delay line receiver (100 Ω adaptation; gain = 2),

(E) the weighted linear mixer (the gain of each channel is adjusted before summation with R7, so that the output amplitude is 2.5 V when E_T = 256 GeV; the amplifier is clamped to limit the saturation), and

(F) the output differential driver.

A photograph of one TBB is shown in figure 11. To correctly form the various analog trigger sums, the values of some components change from one summation circuit to another. These components are R1, C1, R2, C2, R3, R6 and R7. These components have been calculated from Spice simulations validated by measurements (see reference [14] for more details). To cover all the necessary configurations, five TBB versions are necessary: one for EMB, one for the Standard EMEC crates, and three for the Special EMEC crates. The PCB and the design of these five versions are

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identical. The only differences between them are the number of cabled towers (certain towers are not cabled in some cases), the number of channels added in certain towers, and the value of the "variable" components in each tower.

A logic interface is included in the board and devoted to its control and command through the SPAC bus. Four functions are implemented: read/write of the Bimux registers that determine the delay line output used, control of the TBB power supply and temperature, reset of the logic interface itself, and read of the TBB serial number. The logic interface contains four main chips: the TTCRx, the SPAC Slave, the DCU chip, and one Bimux.

Details of the TBB performance can be found in references [14, 15]. Here we summarize a few salient measures as determined on the TBB EMB prototype. The nonlinearity in the linear region (0 V $\rightarrow$ +2.5 V) lies between +0.2% and -0.6%. The maximal crosstalk between towers is 0.8%. The maximal offset value measured at each TBB differential output is 70 mV on positive and negative. The measured noise contribution from the TBB, when limited by the bandwidth of the system, is at least an order of magnitude below the expected preamplifier noise. Each TBB input channel has been tested by injecting a reference signal and comparing the measured amplitude and peaking time with the Spice simulation. The maximal amplitude error is $\pm$1% and the maximal peaking time difference is $\pm$0.4 ns. The differences between measurement and simulation are due to the limited precision of the Spice model, and the 1% precision of R and C components.

The behaviour of the saturation is controlled by using Opamps with clamping at all amplifying stages of the trigger chain. The saturation performance has been verified using three tools: a test bench that reproduces one channel of the trigger chain, one detector module and its electronics during beam tests, and a Spice model of the trigger chain that includes all its channels. The important point is the amplitude finally digitised by the L1CAL ADC, which takes five samples of the Receiver output, separated by 25 ns. Figure 12 plots the evolution of the amplitude of these five samples for increasing injection energies, measured when the signal is injected in one unique cell of the middle EM layer at η = 0.3. Figure 12(a) represents the Receiver output signal versus time for increasing energies. This figure is used to calculate figure 12(b), which represents the amplitude of each of the five samples versus energy. Measurements such as these have been made for many different values of η and layer, and verify that the amplitude of the central sample (line "3") in the saturation region does not decrease below its level at 256 GeV. Of course, when an EM shower occurs in the calorimeter, it induces signals not in only one, but in numerous cells of the four layers. We have simulated this effect with Spice using different shower profiles. The same conclusion is reached, namely that in all cases the amplitude at the chain output is linear up to 256 GeV, and that for even higher energies it does not decrease below its value at 256 GeV.

A total of 135 TBB were produced, while 120 are needed to instrument the full detector. The quality of the boards was controlled during the production. The main parameters to control were the amplitude and the width of the output signals when signals similar to the physical signals of the experiment were injected at the input. Table 3 shows the results of these controls. The gain standard deviation is about 0.5% for each TBB version, and the gain maximal deviation is between 3.2% and 1.5%, depending on the version. This is below the required maximal deviation (5%). Concerning the signal width, the standard deviation is about 0.25 ns and the maximal deviation is around 1 ns. Again, this is below the required deviation (a few ns). Most of these dispersions between boards are due to the 1% precision of the components.

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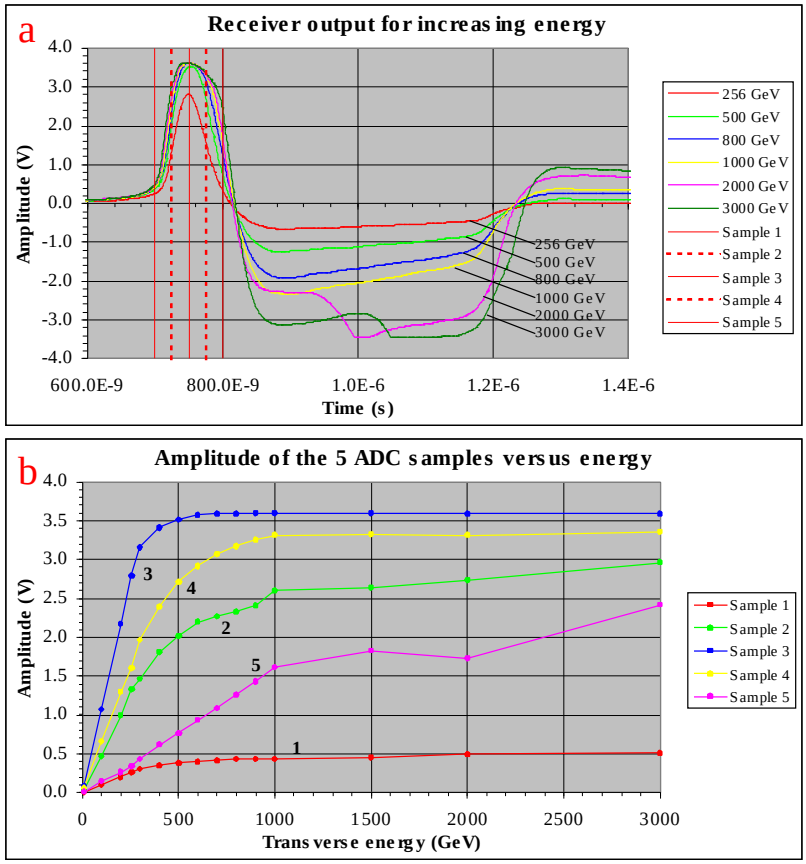

Figure 12. (a) Receiver output signal, versus time, measured for increasing energies on the test bench (the 256 GeV reference signal is shown in bold, and the five sampling times in dotted lines). b) Evolution of the five sample amplitudes versus energy, extracted from the measurements of figure (a).

Table 3. Variations measured on the production TBB boards.

Type		EMB	EC Standard	EC Special 0	EC Special 1	EC Special 2
No. of TBB (incl. spares)		70	35	10	10	10
Gain Error (%)	Std. dev.	0.52	0.55	0.49	0.54	0.50
	Max. dev.	3.05	3.19	2.32	2.39	1.52
Width Error (ns)	Std. dev.	0.26	0.29	0.23	0.26	0.22
	Max. dev.	1.28	1.03	0.70	0.99	0.69

4.2 Tower Driver Board

The trigger sums for the HEC are formed by summing the longitudinal depth segments at the same η, ϕ coordinates. This summation is performed by the shaper chips in the FEB. In contrast to the EM calorimeters, therefore, no further summation of signals is needed for the HEC L1 trigger system. The same is true of the FCAL. Therefore, instead of using a TBB as described

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Table 4. Some of the specifications of the analog performance of the TDB.

Parameter	Specification
Input Impedance	50 Ω± 5%
Integrating Pole	< 2 ns
Crosstalk	< 1%
Gain Variation	< 1% RMS
Integral Nonlinearity	< 1% up to 3 V
Noise Contribution	< 5% of total noise
Output Impedance	44 Ω ± 5%

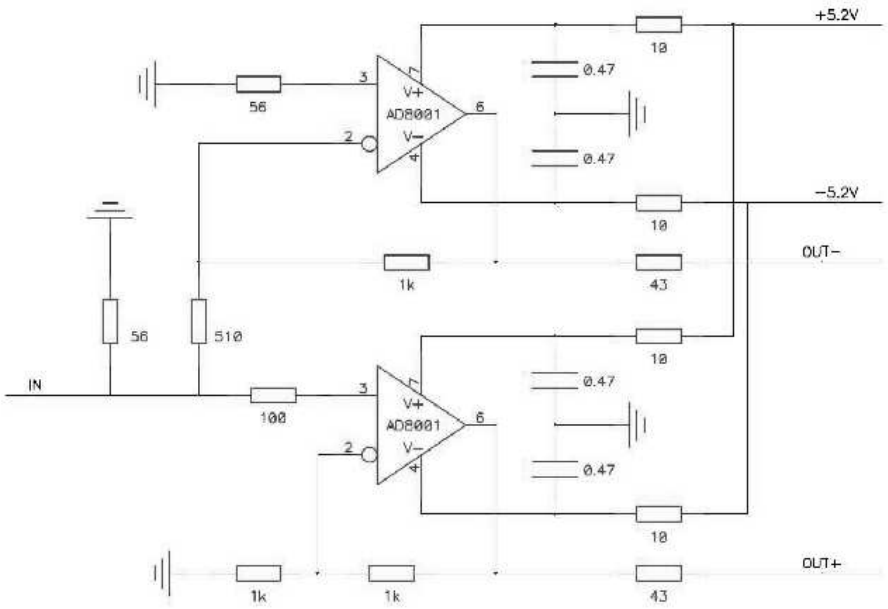

Figure 13. Schematic of one trigger channel as implemented on the TDB.

in the previous section, the HEC and FCAL crates include a TDB. The functions of the TDB are to receive via the baseplane the trigger sums from the LSBs on the various FEBs, convert them into differential signals with approximately unity gain, and drive these differential signals over the 70 m trigger cables to the Receiver system in USA15. Specifications of the TDB performance are summarized in table 4.

A schematic of one trigger channel of the TDB is given in figure 13, showing the single-ended to differential conversion of the trigger signal. The TDB is implemented as a six-layer PCB, and contains 96 channels. A photograph of a TDB is shown in figure 14. The total of 192 amplifier chips are all mounted on one side of the PCB, and placed near the input connectors at the bottom of the figure in order to minimize the trace length for the input signals from the FEBs. The six output cable connectors are mounted along the front panel at the top of the figure. Since the TDB is strictly an analog board, with no external control, the TTC and SPAC signals are not connected

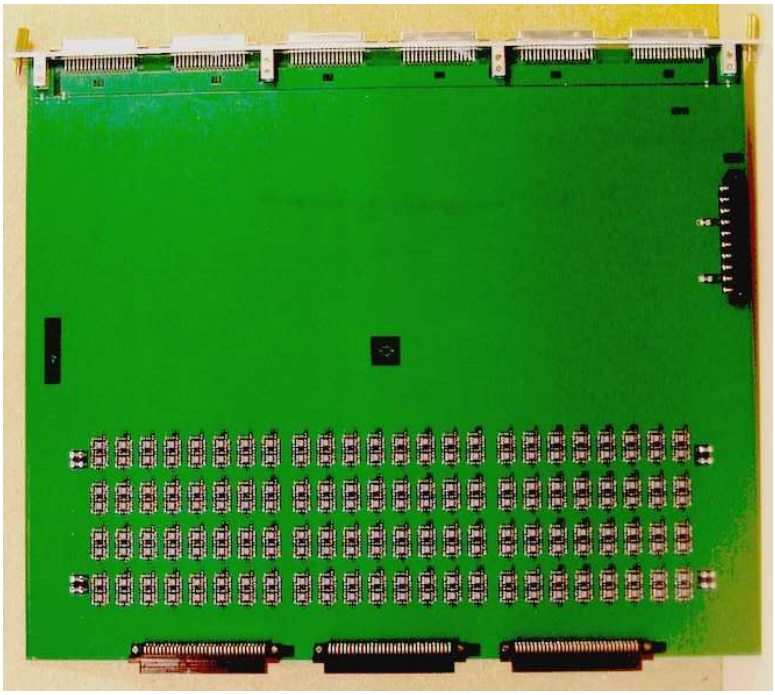

Figure 14. Photograph of the TDB. The pairs of Opamp chips implementing the driver circuit for each of the 96 channels are visible.

to the TDB.

The TDB gain and rise time in response to a step function input were measured for the 96 channels of the preproduction TDB. The mean gain was 0.98 and the channel-to-channel variation of 0.3% is well below the 1% specification. Similarly, the mean rise time of 0.68 ns is well below the 2 ns specification. Sample pulse shapes are shown in figure 15.

The TDB power consumption is very low (< 15 W), so water-cooled cooling plates are not required. Instead, simple aluminum plates are mounted on both sides of each TDB. In addition to spreading the heat, they provide Faraday shielding as well as mechanical protection of the active components.

4.3 Receiver/monitor system

The Receiver system [16] is the electronics at the interface between the FE electronics of the calorimeters and the L1CAL system. The Receivers are located off the detector, in USA15, and are used for both the LAr calorimeters and for the scintillator-tile-based hadronic calorimeter (Tilecal).

There are a total of eight Receiver crates, four on either side of the detector. One Receiver crate is made up of four different type of boards, all in 9U VME mechanics, but as this is an analog system, no VME protocol is used. The system is housed in a standard 9U crate outfitted with a custom backplane. Each Receiver crate includes 16 transition boards, 16 Receivers, two monitoring boards, and one controller board. The transition board, containing completely passive electronics, is a 120 mm deep PCB that is plugged into the back of the crate. The other boards are each 400 mm deep and are plugged into the front of the crate.

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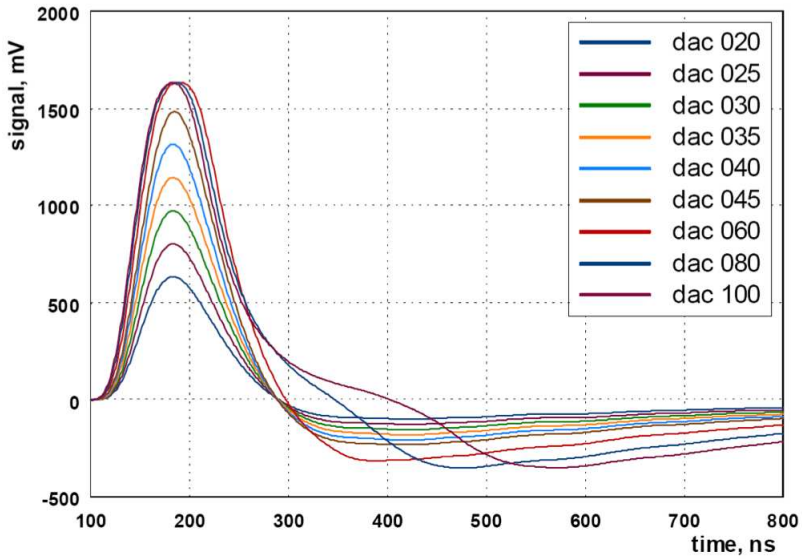

Figure 15. Pulse shapes measured for the TDB for various input signal amplitudes.

The functions of the system include receiving the L1 trigger sums sent from the FECs on long copper cables, adjusting the gains of the various sums, in a few cases performing additional summing, reordering the signals such that they arrive at the L1CAL with the correct mapping, and driving the final sums to the L1 system. In addition, the Monitor part of the system provides pickoffs of the various trigger channels that can be examined using an oscilloscope or other instrumentation.

A schematic diagram of the chain of electronics which accomplishes these requirements is shown in figure 16. The analog trigger signals are sent from the FECs to USA15 over shielded twisted-pair cables, containing 16 pairs each. The trigger cables are plugged into the connectors on the front panel of the transition board which resides in the back of the crate in the slot occupied by the Receiver with which it is associated. The transition boards for three of the four crates are identical, while the transition boards for the EMB have an additional connector to permit four of the input signals to be routed to the EMEC crate. This provision is required since one of the trigger towers is split across the barrel and endcap, and the summing of the two halves of this tower is carried out in the Receiver system. The transition boards use 1:1 wideband stripline transformers to convert the signals from differential to single-ended format. The single-ended and inverted outputs are fed to the Receiver housed in the same slot through the connectors on the backplane.

The signal then enters the VGA (variable gain amplifier) daughterboard, a critical active element in the Receiver chain. Here the signal is inverted again and amplified by a gain to adjust the signal level to its correct amplitude (10 mV=1 GeV at the ADC input). The gain can be varied between zero and two by adjusting the value of a 12-bit DAC which is located on the VGA daughterboard.

At the exit of the VGA daughterboard, the signal, which is bipolar with the first lobe negative, is sent to both the remapping board and to a buffer amplifier in the monitoring branch discussed below. The signal sent through the remapping board becomes transposed in its position among the

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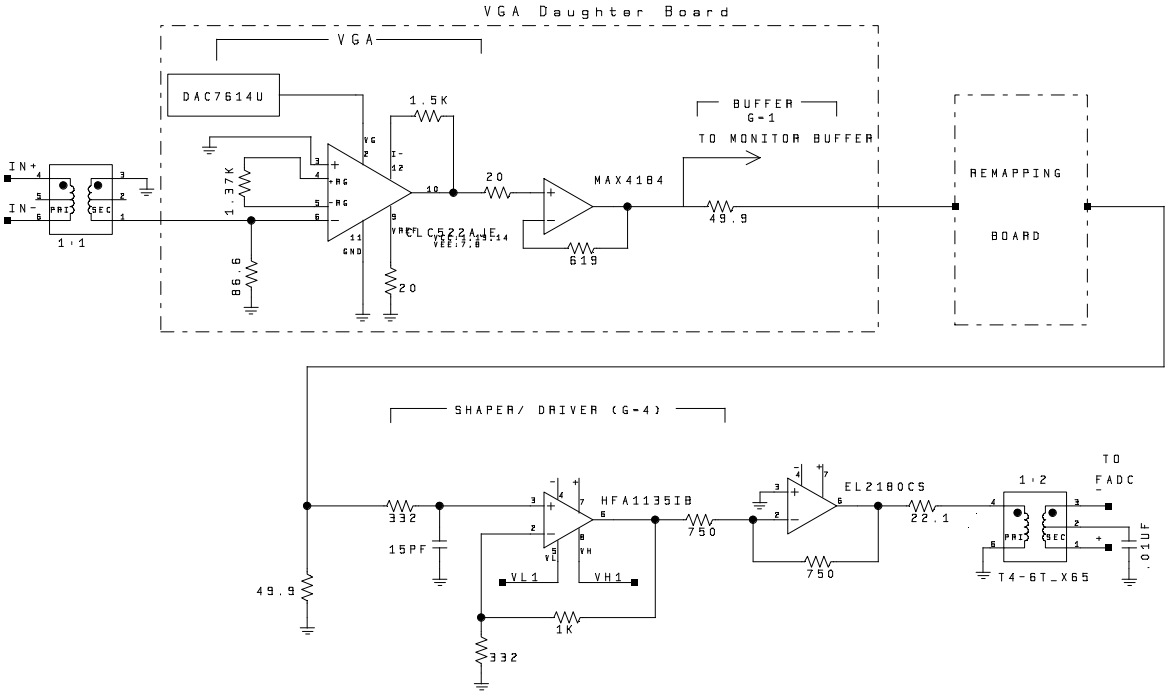

Figure 16. Schematic diagram of the analog circuitry which performs the signal processing for one channel of the Receiver. The trigger sum cable is incident at the upper left, and the output to the cable to the L1 preprocessor is at the lower right.

output signals to the ordering required by the L1CAL. It then undergoes RC shaping (τ=5 ns) to provide bandwidth reduction and amplification by a fixed gain of 2. This factor of two serves as an approximate compensation for the attenuation in the long cables from the detector. The remapping is necessary since signals arrive at the Receiver in an order determined by the physical properties and cabling of the calorimeter, while the L1 logic requires signals ordered in a specific pattern in $\eta - \phi$ space. The mapping of the system is described in more detail in references [17]–[18].

The remapping board [19] is a 253 mm $\times$ 50 mm PCB located in the center of the Receiver motherboard. There are a total of 22 remapping boards defined for the entire system, but in one case, the specifications for two boards (EMB and Tilecal, side A) overlap completely, so the same board serves both purposes. Most of the boards are completely passive, but on six of them (three on each side), twofold sums are carried out:

1. Summing of EMB and EMEC portions of the shared trigger tower. The trigger tower in the region 1.4$< |\eta| <$1.5 is split between the EM barrel and EM endcap, which are in separate FECs. The portions within each calorimeter are summed in the appropriate TBBs, but the sum of the two halves needs to be carried out in the Receiver. This is done by splitting off 4 signals from each transition board in the EMB and bringing them as inputs into the EMEC transition board at the corresponding value of ϕ. Summation is carried out in the remapping board in the EMEC Receiver.

2. Summing of FCAL η bins. The η granularity of the FCAL trigger sums reaching the Receiver is four-fold, whereas the current L1 trigger has only one bin in η. The higher gran-

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ularity may be exploited in the L1 trigger at a later date, but at the start of the experiment, it is necessary to reduce the η granularity ahead of the L1 processors. In the preprocessor, it is possible to create a digital sum of four, but in the case of the hadronic sections of the FCAL (dubbed FCAL2 and FCAL3), an additional two-fold sum is required to add together the two hadronic sections. Thus one level of summing is carried out in the Receiver. Due to the similarity of signal shapes, a sum of neighbors in η is made in the Receiver, leaving the remaining summations to be done digitally.

The final stage of the Receiver electronics chain is a transformer-coupled differential driver. A differential driver consisting of an amplifier and a 1:2 wideband transformer converts the signal back to differential mode (with its original polarity) for transport over twisted pair cables to the L1 preprocessor. The maximum voltage at this point is set by a voltage-limiting Opamp to be 3 V, whereas the range of the ADC in the preprocessor is set to 2.5 V for E_T of 256 GeV. The gain of the circuit consisting of the differential driver on the Receiver and the differential receiver on the preprocessor is unity, so the difference in amplitude ($\approx$ 10%) between the signal level at the Opamp output in the Receiver and that seen by the ADC in the preprocessor is due to attenuation of the $\approx$ 10 m twisted pair cable between the two units and the final RC shaping of τ=5 ns in the preprocessor.

In the main readout, the calorimeter signals are sampled at 40 MHz and digitized in the FE electronics. Thus the only place where analog signals can be examined is in the L1 sums. Monitoring is accomplished in this system by picking off an input signal and routing it into one of 16 monitoring channels. Two monitoring boards, each handling 8 channels, present the output of the monitoring lines on two output connectors, one with shaping identical to the signal output and the other with additional filtering, designed to have sensitivity to different regions of the noise spectrum. The heart of the monitoring circuitry is a crosspoint switch, located physically on the VGA daughterboard. This device routes a signal on one of its 16 inputs to any of its 16 outputs. The four crosspoint switches in a Receiver are bussed together in such a way that any of the 64 channels can be routed to any of the 16 monitoring channels. The signals pass through a buffer amplifier with an output enable. In the monitoring board, the same chip is used to select which of the Receivers are to be transmitted to the monitoring outputs. Enabling the signal at both the source and Receiver ends is not logically necessary, but this arrangement reduces possible crosstalk between the active and inactive monitoring lines in the backplane. The gain in the Receiver chain is chosen to make equal the monitoring signal and the signal on the front panel of the Receiver. Due to attenuation in the backplane, which depends on the position of the Receiver, this equality is accurate only to the level of a few percent.

Each Receiver motherboard has 64 channels, and contains four VGA daughterboards, one remapping daughterboard, and one serial control daughterboard (SCDB). The SCDB sends and receives digital data over the crate backplane. Mounted directly on the Receiver motherboard are the shaper/driver circuitry and the circuitry for driving the monitoring lines, which are located in the crate backplane. A photograph of the Receiver and transition boards in a test bench setup is shown in figure 17.

The system is controlled from a computer via its USB port. The controller board, which resides in the first slot of each Receiver crate, contains two USB ports. One is dedicated to the data

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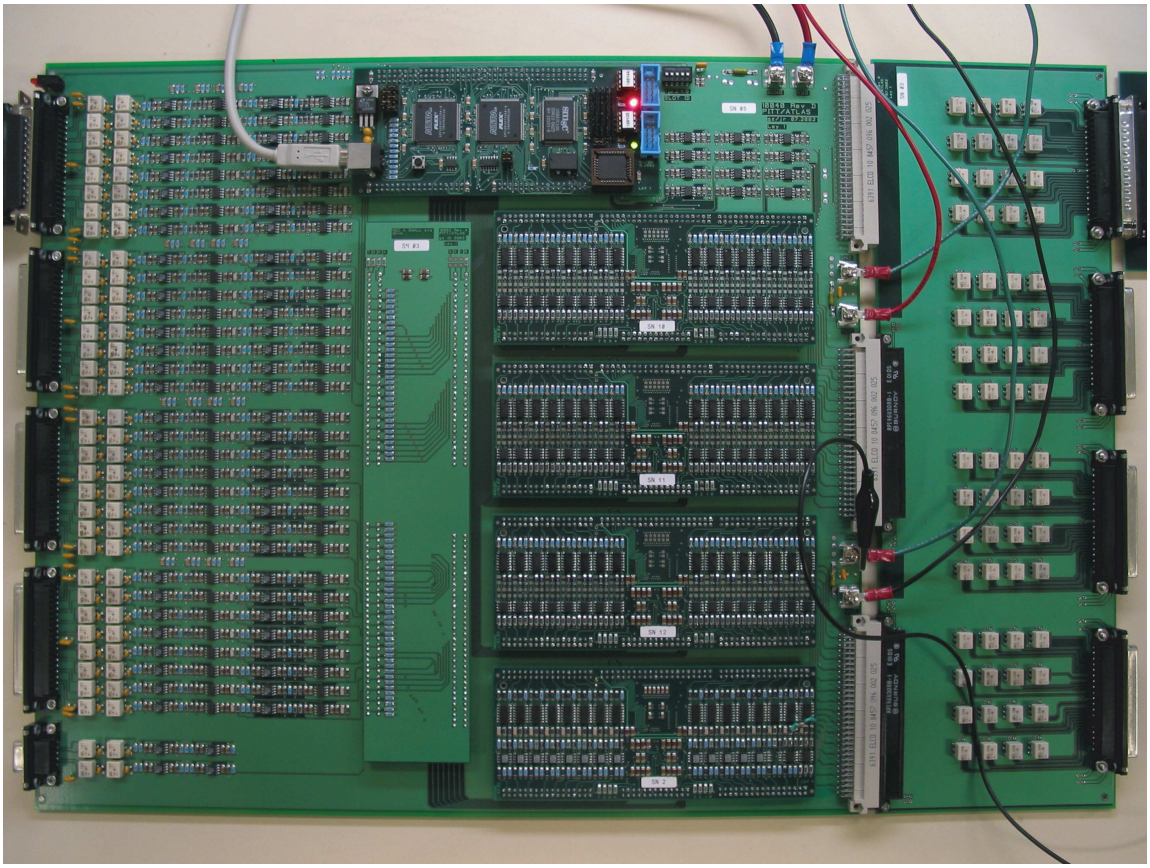

Figure 17. Photograph of the Receiver and transition boards in a test setup. The signals enter on the right side at the front panel of the transition board. The elements through which the signals pass can be identified (right to left) as transition boards, backplane connectors, VGA daughterboards, remapping board, output drivers, output transformers, and output connectors on Receiver motherboard. The SCDB, top center, is a special testbench version with a USB interface, permitting direct control of the Receiver with a computer. Monitoring line drivers are located just to the right of the SCDB.

acquisition system and is the port through which all digital data are transmitted, including gain data as well as monitoring setup data, and identification information is read from the Receivers. The second port is used only for monitoring purposes, and it therefore has a more restricted instruction set available to it. Communications are carried out between the controller and Receiver or monitoring boards using a serial link running at 6 MHz. More information on the digital communications in the Receiver system is contained in reference [20].

Due to the fact that the Receiver must rearrange the order of signals between its input and output, it is of utmost importance that Receivers are placed in the slot for which they were configured and that each board is correctly configured for its slot. For this reason, all daughterboards and the motherboard have been given electronically readable identification numbers.

The backplane in the crate has several functions. The Receiver and monitoring boards each contain three 96-pin connectors which mate with connectors on the backplane. On the Receiver, the two lower connectors transport the signals from the transition board into the Receiver. The upper connector is used to transmit digital signals from the controller to each Receiver over a

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common set of lines, which are carried by the backplane. This connector is also used to transport the 16 monitoring signals out of the Receiver. On the monitoring board, the two lower connectors are used to input the 128 monitoring lines from 16 Receivers, and the upper connector is used for digital communications. The traces in the backplane carry the monitoring signals from the Receivers to the monitoring boards. Power is also distributed over the backplane, using the power bus provided by the crate manufacturer. Analog power for the system is provided by two 100 A power supplies running at $\pm$5 V (one for each polarity). Digital power is provided by an identical but separate +5 V supply. A full crate consumes about 730 W, and is air-cooled in a closed rack with recirculating water-cooled air.

Several automated test stations were set up to evaluate the boards in the Receiver system during acceptance tests carried out at the University of Pittsburgh. A complete discussion of the testing program is contained in reference [21]; here we give the salient results of the more important tests.

The most critical component in the analog chain is the VGA, which has its own test bench where each unit was evaluated thoroughly for dynamic range and linearity. Using a VGA DAC setting corresponding to a gain of about 1.4, a DC signal was ramped at the input from -3.5 V to +3.5 V, and the output was measured on a digital voltmeter to determine the DC response curve and gain for each of the 16 channels. The integral nonlinearity was evaluated separately for negative and positive voltages, since the circuit has a larger dynamic range on the negative side, which gives rise to a lower integral nonlinearity for negative voltages. This is a property of the VGA chip, and is the reason that we have chosen a double inversion of the signal in the Receiver, which results in the leading lobe of the pulse in the VGA chip being negative. The results demonstrate an integral nonlinearity below 0.1% for the negative region, and between 0.2 and 0.3% for positive voltages. The specifications call for a nonlinearity below 1% for the entire electronics chain in the Receiver. The variation of the gain as the control voltage is varied using the DAC on the VGA daughterboard was also measured. This relationship is a linear one, and the behaviour can be quantified as a nonlinearity, but in our application it is not essential that the gain versus voltage relationship be linear, as the gains are set iteratively. The gain nonlinearity is better than 1% over the full range.

One of the more important quantities measured in our acceptance tests is the overall integral nonlinearity of the Receiver circuit in response to pulses. This measurement, carried out with bipolar pulses of 38 ns rise time, simulates closely the situation encountered in the experiment. The results were typically in the range 0.1 to 0.2%.

Another important aspect is the noise which is injected into the system by the Receiver. The noise is dominated by the contribution from the VGA chip which, according to a model given by the manufacturer [22], depends upon the gain of the circuit. Figure 18 shows the measured values of the noise at the output of the Receiver, along with the evaluation of the noise model for our circuit. The dependence on gain is well described by the model, but it gives values which are $\approx$10% higher than our measurements. We view the agreement as reasonable, given that we are operating the chip with very low gain (G=2) compared to common applications. The maximum noise seen in the test (where τ=15 ns) is about 0.5 mV, corresponding to 50 MeV. Reduction of the time constant from 15 to 5 ns increases the noise to about 0.7 mV or 70 MeV. Typical values of noise in the trigger sums are $\approx$ 500 MeV.

Tests of the digital logic of the system were also made in an automated test bench into which was integrated a logic analyzer. Commands were downloaded into the controller, and its output

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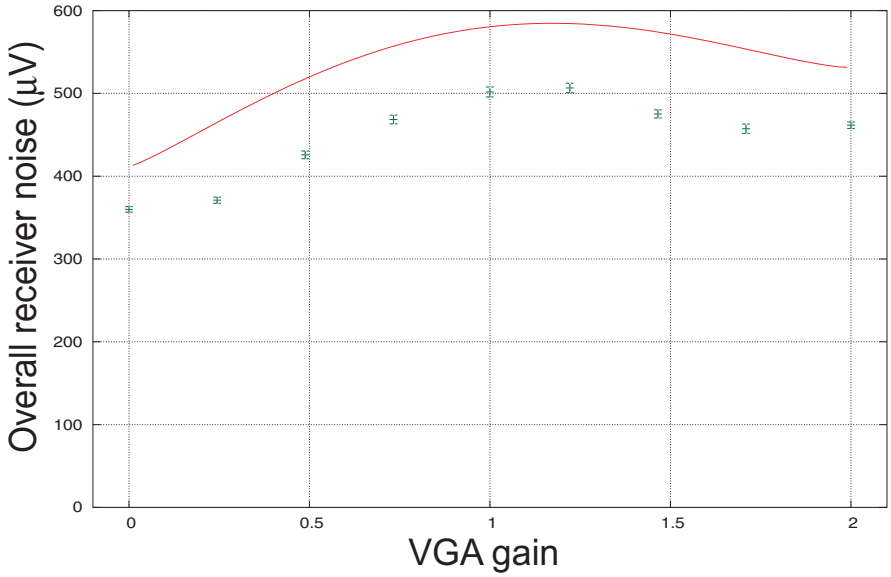

Figure 18. Receiver noise versus gain, as measured with a wideband RMS voltmeter at the Receiver output. The solid curve is an evaluation of the noise model provided by the manufacturer of the VGA chip for our particular circuit.

bit pattern in the internal serial link was recorded in the logic analyzer and compared to a standard pattern, produced by a controller known to be operating properly. Similar tests were carried out for each SCDB.

Tests of two passive components, the remapping boards and the crate backplane, were also part of the test program. The position of output versus input signals was measured and compared with the required mapping. For the backplane tests, a Receiver was moved systematically from slot 6 to slot 21 while automated performance tests were carried out. This test not only checked the proper connectivity of the backplane but also validated the operation of the serial link over the full length of the communication paths in the crate backplane.

5. Front End Crate infrastructure and services

The conceptual design of the FEC infrastructure is shown in figure 19. Photographs of some of the main components of the infrastructure are collected together in appendix C.

The FECs are mounted on top of mechanical structures called pedestals, which serve as transition pieces between the cylindrical walls of the cryostats and the flat crate bottom. The design of the mechanics and of the infrastructure has been conceived to extend the detector's Faraday cage to the low-noise FE readout, maximizing shielding and optimizing grounding paths in order to minimize pick-up and external sources of coherent noise. Inside the pedestal, the calorimeter signals are routed from the feedthrough to the FEC baseplane via stripline cables. The FEC baseplane plays the role of a traditional backplane, except in this application only analog signals are routed on the lines. Power distribution within the FEC is done along one side of the FEC via a dedicated power bus. Another bus mounted on the same side of the FEC is used to distribute the SPAC signals to the

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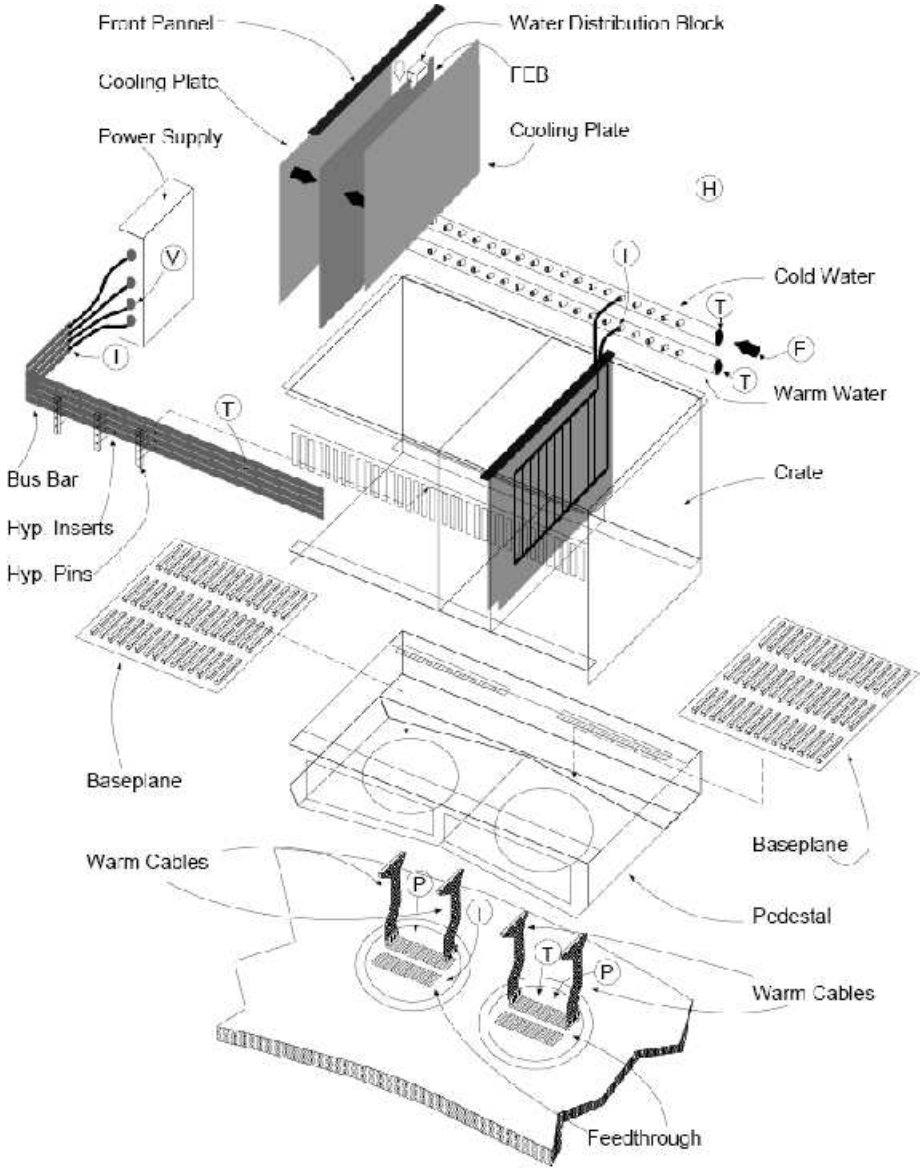

Figure 19. Conceptual drawing showing the various components of the FEC system infrastructure.

various boards in the crate. A LVPS mounted nearby provides the low voltage power to the FEC. Cooling manifolds mounted next to the FEC circulate cooling water through the LVPS and through cooling plates mounted on the FE boards. More details on the various infrastructure components are presented in the following subsections.

5.1 Pedestal and feedthrough services

The pedestal is built as a three-piece welded, relatively soft aluminum alloy construction: the body, the front and the back sections. The body and the back sections are pre-formed in a computer-aided bending machine, while the front part is an aluminum L-profile cut and machined to size. The pieces are then welded by a robotic welding machine. The front-cover door and two support

bars to strengthen the structure and to house the baseplanes are added at a later stage. The built pedestal is finally machined (for example, grooves for RF shielding are created) and submitted to surface conversion coating as per MIL-CC-5541E, Class 3.

Warm cables inside the pedestal connect signals from the feedthroughs to the baseplanes. Each is an assembly of two micros-stripline flexible cables with custom termination at both ends. A 3-row 96-pin connector is used to connect to the baseplane, while a customized 64-pin connector is used to mate with the feedthrough pin-carriers. The cables have been manufactured with two flex circuits to ANSI/IPC-A 600 Rev. E and ANDI/IPC-FC250 RevA specifications, each carrying 32 signals. On the feedthrough side the ground traces are common to the connector ground shield on the corresponding side of the connector. However the ground shields are isolated from each other and shorted together only when inserted into the pin-carrier. The trace widths for signal and return paths are respectively 205 and 357μm. The corresponding line impedance is 33$\Omega \pm 10\%$, with electrical lengths equalized to a maximum of 50 ps delay spread. A photograph of one warm cable can be found in appendix C.

In addition to the signal cables, the pedestals also house feedthrough services for vacuum and temperature control. Feedthroughs are evacuated separately from the high vacuum system for the insulating volume between the two cryostat vessels. Two switchable vacuum lines on each feedthrough, controlled by pneumatic valves, allow separate pumping on any feedthrough which may develop leaks, without compromising the vacuum in the other feedthroughs. The valves are sensed by double-position micro-switches and connected to the cryogenics monitor system. Furthermore since the vacuum cables connecting the cold and the warm flange in the feedthrough would cause heat conduction leaks and potentially condensation and frosting on the outer flange of the warm flange, heater elements (50 W max.) are installed on the flange together with sensors to monitor the temperature of the area. The wire needed to operate the heater elements is routed through the pedestal. A Filter Box provides ground loop isolation for the feedthrough services installed in the pedestal. It implements a low-pass second-order filter, which is required for any penetration in a Faraday cage that shields high sensitivity low-level signals like the ones from the LAr calorimeters. Technical details on the circuitry, the implementation and the integration underneath the pedestal structure are available in reference [23]. A photograph of an empty pedestal mockup, showing the position of the vacuum lines and the pneumatic valves, can be found in appendix C.

5.2 Front End Crate mechanical assembly

The FEC chassis is constructed using sheet-metal technology in two stages. First the outer shell, providing the necessary rigidity, is built as two L-shaped interlocking parts. An inner layer is then installed with card guides spot-welded from the inside. During installation of the FECs on the pedestal, the FEC is first aligned by a set of dowel pins on the pedestal. Two mini-skirts are used to secure the FEC to the pedestal. Then the FEC is bolted to the pedestal top surface with a set of M3 screws at 10 mm spacing. To improve shielding and ohmic contact between the pedestal and the FEC, RF gasket material is applied in the grooves machined on the pedestal.

Undesired noise currents on the FEB or noise picked up from external sources could deteriorate the performance of the readout, particularly considering that the energy of many cells have to be summed. These currents have to be diverted as much as possible from the FEB inputs to the FEC body and from there to the cryostat. This can be achieved effectively by providing a very low

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impedance connection between the FEBs and the baseplane ground layers and also to the FEC itself. The baseplane design is described below. The connection to the FEC is managed through an optimized design of the FEB front panel. Conformally coated "cleats" screwed into the FEB anchor the panel to the board and provide a good ohmic contact with the FEB ground planes. The front panel includes captive screws to tighten and connect the FEB to the FEC; they also serve as jack-screws to disengage the connections at the baseplane while extracting the board. RF gaskets mounted on machined grooves on the side of the front panel provide connections from board to board, minimizing penetration in the crates and effectively realizing a complete RF shield on the FEC top surface. These connections extend the Faraday cage of the cryostat up to the top of the FEC.

5.3 Power bus

The power distribution to the FE boards is mounted along one side of the FEC. This scheme differs from typical schemes in communication and data aquisition busses, where power and signal lines are routed on the same backplane. Such a choice was driven by the sensitive low-level analog signals entering in the FEC along the FEC baseplane and the need to minimize noise pick-up through parasitic couplings.

To manufacture a power bus, the copper bars are cut to size and pre-bent. The material used is 110 copper alloy with a 12.74 mm^2 cross-section, dimensioned to carry up to 200A. The copper bars are then terminated with connectors. Next the bars are bonded together with epoxy on a appropriate fixture. Aluminum mounting bars are also glued in the process. The front and back of the bussbar are covered with thin G10 plates that also serves as a safety guard. After the curing process the bussbar is mounted on a numerically-controlled milling machine for drilling. Knurlet sockets are finally press-fitted and provide pass-through connections. Ten-pin power combs are inserted through the bussbar to connect power to the various FE boards. The contacts are rated for 10 A and have nominal resistance of 2.5 mΩ. At the maximum current foreseen, a temperature increase of 10° C above ambient temperature is expected. An assembly drawing and a photograph of a power bussbar mounted on an FEC can be found in appendix C.

5.4 SPAC bus

The SPAC bus consists of a PCB attached on one side of the FEC. The connection between the PCB and the FE boards is achieved by inserting a comb with pins that traverse through the SPAC bus PCB and into a connector on the receiving board. This design enables removal of a single electronic board from the FEC without needing to disconnect all the connections.

Most of the FE crates are equipped with two 19-position SPAC buses, one bus covering slots 1 to 19 and the second slots 20 to 38. However, the special EMEC/HEC FEC contains three 12-position buses. The two identical left and right buses cover slots 1 to 12 and 25 to 36, respectively. The middle bus covers slots 13 to 24, and differs from the left and right buses by the gap between slots 19 and 20, which is larger than the standard pitch of the other slots due to the central mechanical support of the FEC. To equip all of the FE crates, 98 SPAC19 standard buses, 16 SPAC12 buses and 8 SPAC12 middle buses are required.

The buses are 1.6 mm, four-layer stripline PCBs. The four differential SPAC signals are routed on the two inner layers and enclosed between two ground planes. The lines are terminated in 100 Ω

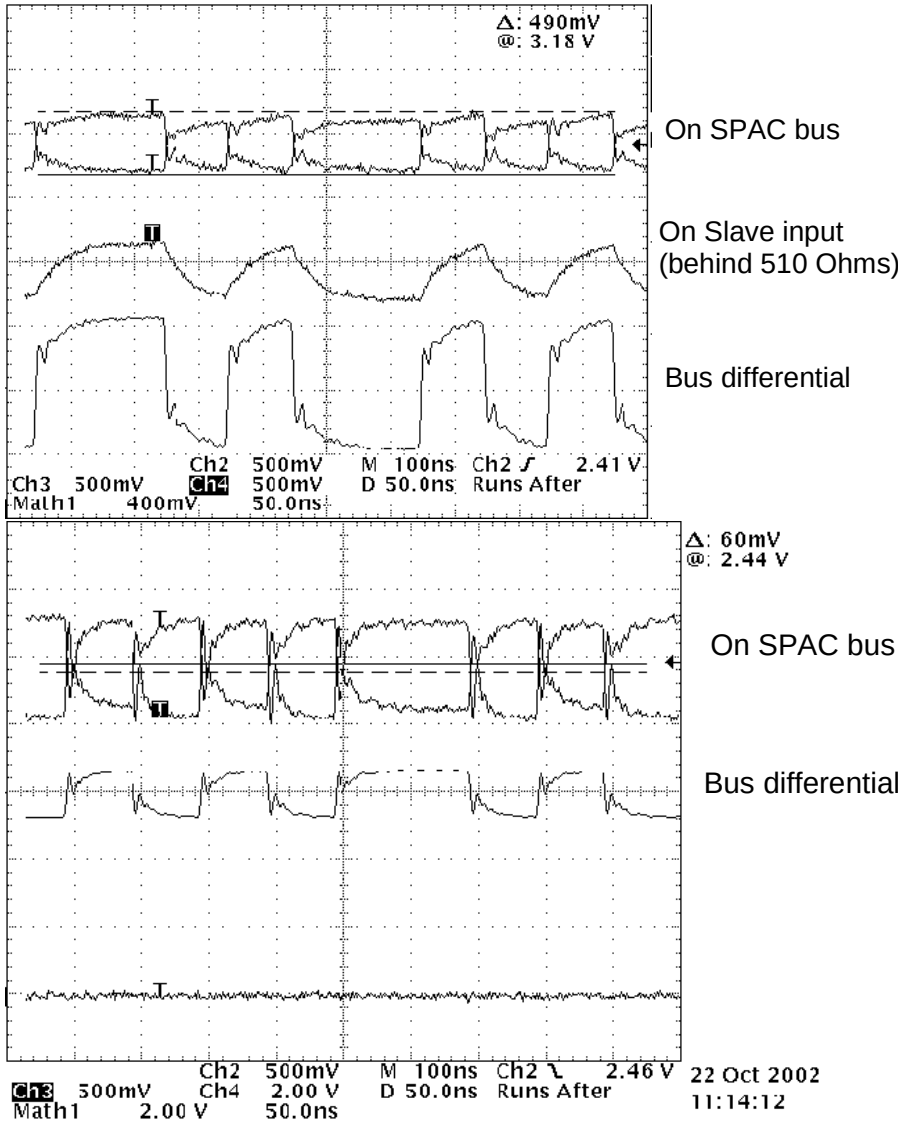

Figure 20. Measurements of a MS1 download line (upper figure) and of a SM1 readback line, in each case for a fully loaded 19-slot SPAC bus.

on both ends of the bus. The bus PCBs are not directly screwed on the FEC frame, but through copper spacers which are soldered on the PCB, in order to guarantee a gap between the bus and the FEC frame and to make a good ground connection between the bus and the FEC. More details on the connections between the SPAC ASICs and the bus are given in reference [9]. During the design phase, simulations of the bus performance were done to validate the reliability of the bus. The results were also verified by measurements on the SPAC19 bus prototype. The bus was integrated into a system containing a SPAC slave ASIC configured in repeater mode (as on the Controller) and several SPAC Slaves configured as standard slaves. Some passive loads were also added to the bus to simulate a partially or fully loaded FE crate. The results can be found in reference [24].

Prototypes of the SPAC19 bus were also installed on a FEC in BNL for system tests. Figures 20 and 21 are a few plots of the measurements performed on the bus. The measurements have

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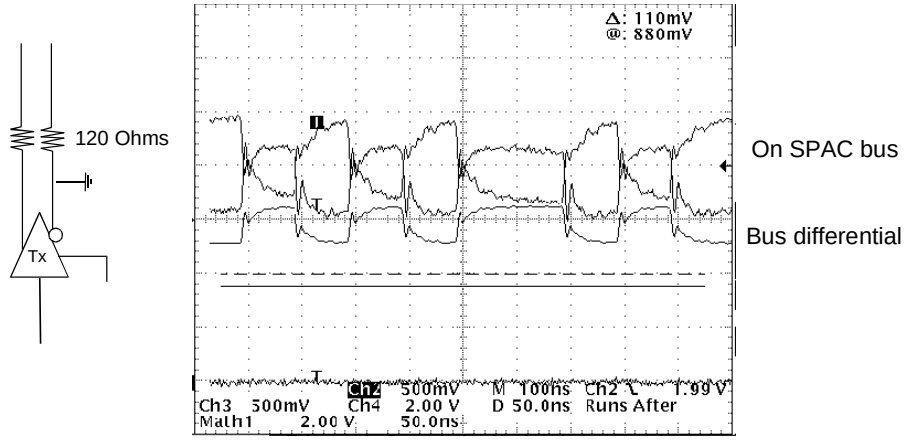

Figure 21. Measurements of a SM1 readback line for a fully loaded 19-slot bus, with one line forced to ground. Even in this serious failure mode, 75% of the frames are read back without errors.

confirmed a good communication with all the boards on a partially or fully loaded bus. As one example of tolerance to failures, the ability to communicate was verified on both the download and the readback lines with one board, even when all other boards are in power failure conditions. Some worst-case conditions were also tested. For example, figure 21 shows the measured signals when one of the signal pairs is shorted to ground on one Slave output on the readback bus, causing the signal pairs to be unbalanced; even in this case, communication could still be performed, with a 75% success rate.

5.5 Baseplane

The FEC baseplane is mounted at the back of the crate, much like a traditional crate backplane. It is a PCB containing three rows of 96-pin connectors which mate with the connectors on the various FE boards. Each FEC uses two baseplanes, except for the FCAL crate which is only half-instrumented. A photograph of an EMB baseplane can be found in appendix C.

The main functions of the baseplane are to provide mechanical support and guidance via alignment pins for the boards in the FEC, to provide an electrical interface between the warm cables in the pedestal and the FEBs, to shield the warm cables from noise radiated from the FEBs, and to transport the trigger sum components from the FEBs to the TBB or TDB mounted in the same HFEC. In addition, the minimization of coherent noise in the readout requires an excellent ground connection between the FEBs and the baseplane. Custom designed gold-plated shields mounted around the FEB input connectors mate with custom manufactured springs soldered on the baseplanes to provide low contact resistance and low inductance when the FEB is installed. In addition, high current gold-plated pins on the FEB mate with corresponding sockets on the baseplane to lower the impedance path to the baseplane ground at the edges of each input connectors, diverting noise currents away from the sensitive inputs. These precautions, plus those described previously, allow the system to reach effectively and systematically coherent noise levels per channel of less than $\approx 2\%$ of the total noise per channel. Figure 22 show a photograph detailing the connections between the FEB and baseplane with the FEB installed in the FEC.

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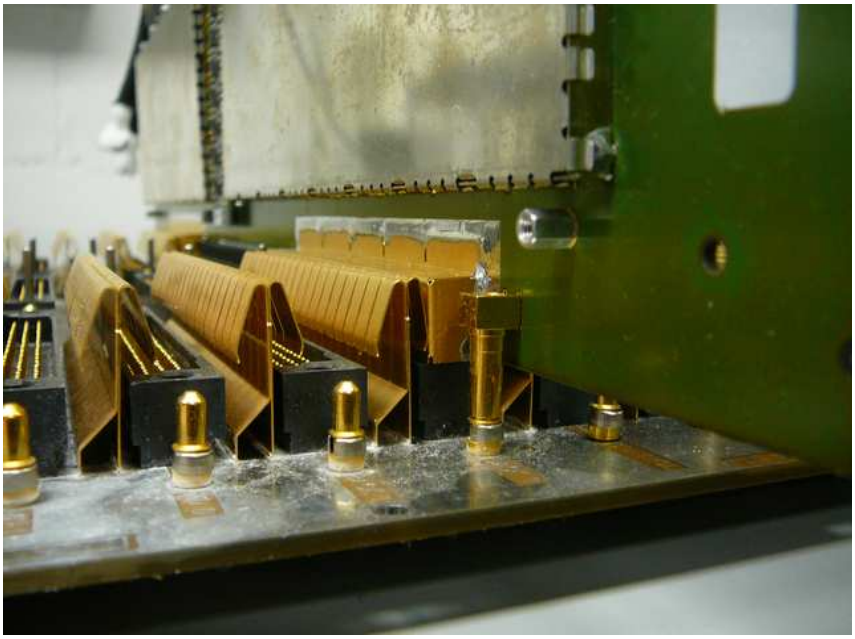

Figure 22. Electronics boards installation in the FEC and details of the connections to the input connectors.

As shown in figure 23, there are four different configurations of FECs, which employ five different types of baseplanes. The mapping of the L1 signals out of the FEBs is determined by the cabling from the calorimeter electrodes to the FEBs. The order of the L1 signals out of the TBB and TDB is determined by the layout of the baseplanes. The mapping is documented in detail in references [25] and [26] for the EMB/EMEC and for the HEC/FCAL, respectively. The routing of the trigger signals in the baseplane requires care to minimize signal distortions and crosstalk, and to avoid the introduction of oscillations. The impedance of all signal lines is specified at $50\pm2\ \Omega$. Routes were chosen to avoid capacitive coupling between the trace and the input of any preamp whose output contributes to the sum being routed. The pinout patterns on the connectors on the FEBs, TBBs, and TDBs were chosen mainly to minimize crosstalk, and are shown in figure 24.

The FCAL baseplane has an additional feature not found in the other baseplanes. Since the calibration signal for the FCAL is not sent to the electrodes, as is done for all other calorimeters, it is necessary to distribute the calibration pulse at the entrance of the signal to the FEBs. This is done by separate PCBs mounted underneath the baseplane. The FCAL calibration signals therefore have a somewhat different nature than those for the other calorimeters and need to receive special treatment in the analysis.

As part of the verification process for the prototype baseplanes, electrical tests were carried out at BNL and the University of Pittsburgh. Continuity checks were made for each of the traces in the baseplane. The impedance of the signal lines was measured using a Time Domain Reflectometer for a few cases and verified to be within the specifications. To check for possible shorts or other anomalies, the capacitance of each trace was measured and plotted against its length. No anomalies were found in any of the baseplanes.

Crosstalk is an important parameter for the trigger system. One of the trigger conditions is an isolated high energy EM shower. Isolation is determined at L1 by examining pulse heights in

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Slot	EM Barrel	EC Standard	EC Special	FCAL
1	FEB PS		FEB PS	CALIB
2	FEB FR 0	FEB PS	FEB FR 0	CAL SHAP
3	FEB FR 1	FEB FR 0	FEB MID 0	FEB F1 0
4	FEB FR 2	FEB FR 1	FEB MID 1	FEB F1 1
5	FEB FR 3	FEB FR 2	FEB FR 1	FEB F1 2
6	FEB FR 4	FEB FR 3	FEB FR 2	FEB F1 3
7	FEB FR 5	FEB FR 4	FEB FR 3	TDB 0
8	FEB FR 6	FEB FR 5	FEB FR 4	FEB F1 4
9	TBB A	TBB B	TBB 0 C	FEB F1 5 E
10	CONT	CONT	CONT 1	FEB F1 6
11	FEB BK 0	FEB BK 0	FEB BK 0	FEB F1 7
12	FEB BK 1	FEB BK 1	FEB MID 2	CONT
13	FEB MID 0	FEB MID 0	FEB MID 3	FEB F2 0
14	FEB MID 1	FEB MID 1	FEB FR 5	FEB F2 1
15	FEB MID 2	FEB MID 2	FEB BK 1	FEB F2 2
16	FEB MID 3	FEB MID 3	TBB 1	FEB F2 3
17	MON	MON	FEB MID 4	TDB 1
18	CALIB	MON	FEB MID 5	FEB F3 1
19		CALIB	FEB L1	FEB F3 2
20	FEB PS		TBB 2	MON
21	FEB FR 0	FEB PS	FEB L2	
22	FEB FR 1	FEB FR 0	CALIB 0	
23	FEB FR 2	FEB FR 1	CALIB 1	
24	FEB FR 3	FEB FR 2	CONT 2	
25	FEB FR 4	FEB FR 3	FEB 1	
26	FEB FR 5	FEB FR 4	FEB 2	
27	FEB FR 6	FEB FR 5	TDB 1	
28	TBB A	TBB B	FEB 3 D	
29	CONT	CONT	FEB 4	
30	FEB BK 0	FEB BK 0	FEB 5	
31	FEB BK 1	FEB BK 1	TDB 2	
32	FEB MID 0	FEB MID 0	FEB 6	
33	FEB MID 1	FEB MID 1	MON	
34	FEB MID 2	FEB MID 2	CONT 3	
35	FEB MID 3	FEB MID 3	CALIB	
36	MON	MON	LV	
37	CALIB	MON	LV	
38		CALIB	LV	

Figure 23. Configurations of the different FEC baseplanes. The columns are labelled by FEC type, and the slot number is shown in the first column. Entries in the table show the type of module, for which the following abbreviations are used: PS=Presampler, FR=Front Section, MID = Middle Section, BK = Back Section, L1 = First section of EMEC Inner Wheel, L2 = Second Section of EMEC Inner Wheel, F1, F2, F3 = FCAL1, FCAL2, FCAL3, MON = Monitor Board, CONT= Controller, CAL SHAP= Calibration Shaper (used for FCAL calibration), LV= HEC low voltage distribution board. All FEC except those for the FCAL contain two baseplanes.

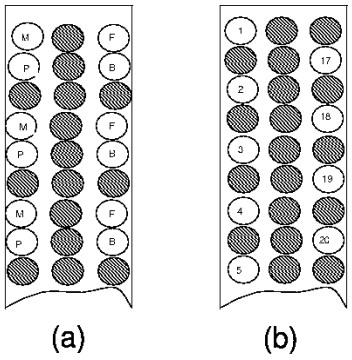

Figure 24. Signal patterns used in the 96-pin L1 connectors in the baseplane. The shaded pins are connected to ground. Figure (a) shows the pattern used at the TBB input, with the pins labelled P, F, M and B corresponding to the four depth layers (Presampler, Front, Middle, Back) for a trigger tower. A row of grounded pins is placed between each group to reduce crosstalk between trigger towers. Figure (b) shows the pattern used on the TDB input as well as the FEB output. To reduce crosstalk between signals, each pin carrying a signal is surrounded by grounded pins.

trigger towers which are neighbors to the trigger tower of interest, and crosstalk to such a tower would reduce the sensitivity to detect such showers. Since the maximum pulse height considered at L1 is 256 GeV and isolation thresholds are set at a small multiple of the noise, typically 0.5 GeV,

crosstalk values of more than ≈ 2 GeV induced by a 256 GeV signal would be problematic. For this reason the maximum permissible crosstalk for the entire analog chain for the Level 1 trigger has been set at 1%. A study of the crosstalk was carried out for the EMB baseplane. In this study, the trace representing the middle layer of a given trigger tower was excited with a 3 V pulse of rise time 38 ns, similar in shape to calorimeter signals. An analog sum of the four layers for all other trigger towers was then displayed on an oscilloscope, and the peak-to-peak amplitude determined. The typical waveform resembled a derivative of the exciting pulse, as expected for capacitive coupling between the traces. The maximum crosstalk value was determined for each trigger tower as the ratio of the maximum value of the signal in the channel in question divided by the amplitude of the source signal. In no case did this ratio exceed 0.2%. Due to the nature of derivative coupling, the first-order effect of the crosstalk is to shift the timing of the pulse rather than its amplitude, so the effect of baseplane crosstalk in the amplitude is completely negligible.

5.6 Optical cables

The digital readout data from the FEBs is transmitted to the BE electronics via multimode optical fibers. The fibers need to traverse the experiment and must be sufficiently protected against mechanical damage during both installation and later handling of nearby detector components. The detector endcaps must be retracted for access to the inner components of ATLAS, and therefore the optical fibers must be routed on flexible cable trays that allow bending without damage and with minimal light attenuation. Furthermore, the fibers must tolerate the radiation environment near the FE electronics, where the first few meters of fibers pass. To assure simple installation and robustness, the fibers are grouped into an optical cable with four ribbons of 12 fibers each. The cable is split into individual fibers near the FE and BE electronics.

The fibers used are Draka (previously Plasma Optical Fibers) HiCap 50 μm core with graded refractive index. These fibers have been shown [27] to withstand the expected radiation levels with less than 0.1 dB/m attenuation. To produce the cables, the fibers were assembled into 12-fiber color-coded encapsulated-type ribbons with a thin outer layer. Four of these ribbons were then inserted into a sheath made of a halogen-free flame-retardant thermoplastic compound. The sheath has an outer diameter of 9.5 mm and a 4×5 mm^2 rectangular hole for the ribbons. To prevent bending in the plane of the ribbons, two glass-fiber reinforced polyester rods are included in the sheath. Details about the cable, developed by the Ericsson Network Technology company for use at the LHC, can be found in reference [28]. While the cable is specified for a pulling force of 800 N, tests showed no significant attenuation up to 2 kN. The maximum fiber strain is 1.1 kN. Crush tests using a 100 mm diameter plate showed attenuation above 2 kN force. Bending the cable 360° showed no loss for radii above 100 mm, while losses were noted for smaller radii. For bends below 180° no attenuation was observed down to 80 mm bending radius. A photograph of one optical cable can be found in appendix C.

Connection to the FEB and the ROD boards are made by individual fibers using ST connectors. To achieve a centering of the fiber within 1 μm the ST connectors used single-mode ferrules. The split of the cable into individual fibers at the FEC side is made in a stainless steel box equipped to provide strain relief for the cable sheath as well as the split fibers. At least 12 fibers out of 48 per cable are reserved as spares. For logistics reasons, the cables had to be installed from the detector side without the connectors at the BE side. To allow testing of cables prior to installation, the cables

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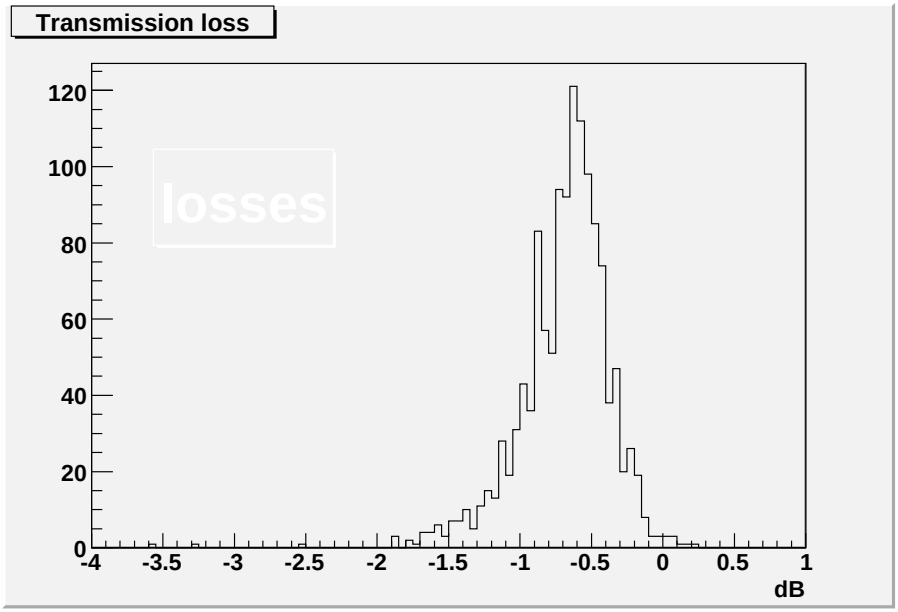

Figure 25. The measured transmission loss for optical fiber pairs. See the text for details.

were delivered double-length with connectors at each end. At installation time the cables were cut into two according to the required lengths. Each ribbon was subsequently spliced onto a ribbon which was split into individual fibers. After splicing, the transmission loss was measured for pairs of fibers connected together at the FEC side. The measured loss for 1296 fiber pairs is shown in figure 25. The average loss is -0.69 dB. Only five fibers were found to have losses exceeding 4 dB, for which spares were substituted. Two fibers were broken at the BE side during installation.

5.7 Cooling distribution

Cooling is required to remove the $\approx$ 800 W dissipated in each LVPS and the $\approx$ 3.2 kW dissipated by the FE boards in each FEC. Given the space constraints, the magnetic field in the FEC regions, and the requirement to not disturb other nearby detector systems, air cooling is not practical. Instead, a water cooling system is employed. To avoid leaks, the cooling water is circulated at an under-pressure, $\approx$600 mbar below atmospheric pressure. Small leaks will, therefore, lead to air migrating into the cooling system, rather than to water leaking out. Since the cooling is conductive, water-cooled heat exchangers need to be placed in contact with active components to remove the dissipated heat. Given the space constraints, plus the desire to minimize the presence of high atomic number material, most of the cooling infrastructure is manufactured from aluminum, which requires special care when bonding, welding, etc.

The coolant circulator is designed to provide water below atmospheric pressure at around 18° C. A distribution manifold distributes the water to the detector, with a distribution network divided into 24 sectors, 12 for the EMB and 6 for each EC. In gaps between the so-called “fingers” at the ends of the Tilecal, the cooling lines branch in two, one for cooling the LVPS unit and one for the full FEC loaded with FE boards. Close to the FEC chassis, two sets of extruded aluminum manifolds, housing 38 quick disconnects, distribute cooling water to the individual FE boards in the

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FEC. Each water-cooled FE board has cooling plates mounted on both sides. An injection-molded cooling block is used for connecting the rubber water hoses from the water distribution manifolds to the cooling plates of the individual FE boards. The cooling plates are attached to the FE boards on aluminim stand-offs that establish a distance of 6 mm from the board surface to the cooling plate.

Corrosion of the aluminum cooling plates is a concern. While oxidation by itself is beneficial to aluminum, since it passivates the surface by creating an oxide layer, water contaminants can easily cause severe corrosion in a relatively short period of time. Chemical surface conversion is widely used to prevent corrosion, but tests with chemically active water (with chlorine) showed this type of treatment is not adequate for our application. Microscopic analysis showed that microfissures introduced during hydroforming of the plates cannot be protected by chemical treatment. The surface also becomes too smooth for bonding purposes. Instead, the cooling plates were first processed through a bio-degradable slightly acidic solution to neutralize chemically active screen-printing components. Natural oxidation was then allowed to form a passive oxide layer. Finally a deionizing filter was installed into the water cooling circuit to keep the water conductivity below 1 μSv/cm (and above 0.5 μSv/cm to avoid chemical activation of the water). During detector operations water needs to be circulated continously to prevent pressure buildup inside the water channels, due to release of hydrogen gas formed during the chemical reaction of aluminum with water.

The gap between the cooling plate and the active components on the FE boards is compensated by heat transfer plates made of aluminum sheets, cut in size and drilled consistently with the standoff patterns on the FEBs. The sheets are hydroformed on a mold derived by three-dimensional models of each side of the FEB. Silicone-based thermal pads impregnated with aluminum oxide are used above highly dissipating components on the board. The material has a thermal conductivity of $\approx$1 W/m-K (300 times lower than aluminum) but it is an excellent electrical insulator, which is the reason it is used to couple active components to the heat transfer plates. Photographs of a cooling plate and a heat transfer plate can be found in appendix C.

Compressed air controlled valves make it possible to operate only certain sectors of the cooling distribution network if needed. Manual valves and overpressure safety valves are installed on the input lines. A PLC (Programmable Logic Controller) is used for pressure regulation (achieved by controlling the opening of each of the 24 sectors' outlet valves) and continuous monitoring of the vacuum, water level and other important operating parameters. In case any of these parameters goes out of the allowed range, the PLC places the cooling system into a "safe" mode (stopping the main circulation pump, closing the inlet valves and opening the return valves to the negative pressure in the top of the reservoir) and generates a hardware interlock to the LVPS system.

5.8 Monitoring system

The FE electronics system is equipped with a FEC and LVPS Monitoring System (FECMS). The FECMS is based on the Embedded Local Monitoring Boards (ELMB) designed and produced by CERN [29], with one ELMB installed for each FEC. The ELMBs are read out and controlled through a Controller-area network bus (CANbus).

The FECMS monitors individually the seven LVPS output voltages on the FEC power bus distribution, as accessed via a Crate Monitoring Board (CMB) installed in each FEC. The FECMS also monitors the LVPS status signals, baseplate temperature and the temperature shutdown override control as described in section 6. In addition, the FECMS measures temperatures via four

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PT-100 thermistors installed in the water cooling distribution circuit for high precision monitoring of the inlet and outlet water temperatures in both the FEC and the LVPS branch of the circuit. Each sensor uses a four-wire readout to achieve relative precision better than 0.1° C. There is no flowmeter installed in the cooling distribution but indirect information can be retrieved by measuring the inlet-outlet ΔT and its trend curves. The FECMS controls the LVPS ON/OFF state through the 280 V supplies. More details about the FECMS are presented in appendix B.

6. Low voltage power supplies and distribution

The low voltage power required by the FE electronics is delivered by a LVPS and distribution system made of 58 identical partitions which are monitored and controlled through the FECMS system. AC-DC primary power supplies (PS), fed from the 400 VAC three-phase network in the ATLAS pit and organized in racks in USA15, deliver 280 VDC and 10-11 A to LVPS made of DC-DC converters mounted on the detector adjacent to the corresponding FEC. One-to-one connections between the 280 V supplies and the LVPS are made via 70-100 m long cables. The low voltage outputs of the LVPS are delivered via 10 2/0 AWG wires ($\approx$ 1.5 m long) to the power bussbar mounted on the FEC. As discussed in more detail in section 8, special care has been taken in the system design to avoid introducing ground loops.

6.1 280 V power supplies

The 280 V supplies were supplied by industry [31]. Their main specifications are listed in table 5. The 280 V PS are housed in closed racks in USA15, eight units to a rack. Each rack has a closed-loop ventilation system with a turbine on top of the rack. Air is forced through ducts along the sides of the racks and then deflected up through the PS. Fan trays below each PS enhance the air flow. The heat is removed by air/water heat exchangers using medium temperature ("mixed water") cooling water provided for the experiment. As discussed earlier, the PS are controlled and monitored by the FECMS. In addition, each 280 V supply is interlocked by a fast hardware signal which turns the units off in case of an alarm (such as cooling water failure, smoke detection in the FE area), independently of software processes.

The racks are part of the general ATLAS infrastructure and are remotely controlled (on/off power) and monitored (temperature, smoke) by the ATLAS Detector Control System (DCS) [30]. The racks are equipped with a fire extinction system using CO_2 release in the closed rack volume. A photograph of racks of 280 V PS in USA15 can be found in appendix C.

6.2 Low voltage power supplies

The LVPS unit is a set of DC-DC converters that convert the 280 VDC into seven low voltage outputs to provide power to the FE electronics. Table 6 shows the voltages, the maximum current, power, and the number of modules with which the LVPS units are built. For improved reliability, the LVPS implements an (N+1) redundancy scheme: while all of the 27 modules are initially active, in the event of the failure of a single module in a voltage rail the remaining modules will still be sufficient to supply the required current. The voltages are trimmed to the required values at 80% of the maximum current, which represents the expected full load of an EMB FEC, the most power demanding configuration. The current values include a 25% growth factor to allow for possible

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Table 5. Specifications for the 280 V AC-DC power supplies.

Parameter	Value	Unit	Condition
Input Voltage	400 $\pm$40	V rms	
Phases	3 + N	-	Balanced
Frequency	47-63	Hz	
Inrush Current	$\leq$ 35	A peak	
Input Power	$\leq$5.5	kW	Operating at full load
Powerfactor	$\leq$ 0.95	-	
Output Voltage	280 (+20 / -0)	V	output terminals
Voltage Adjustment	-	-	Not required
Output Current	$\leq$16	A	
Load Regulation	$\leq$ 100	mV	Load varied from 0 $\rightarrow$ 100%
Line Regulation	$\leq$ 100	mV	Line input varied by $\pm$15%
Efficiency	$\geq$ 85	%	Load range 10 $\rightarrow$ 100%
Ripple and noise	$\leq$ 500	mV p.p	f $\leq$ 10MHz
Voltage rise time	$\geq$150, $\leq$300	V/s	At start up or Interlock enable

Table 6. Output voltages and currents of the LVPS units.

Terminal Number	Voltage [V]	Maximum Current [A]	Maximum Power [W]	Number of Modules	Average Power per Module [W]
2	6.0	100	600	5	120
3	11.0	20	220	2	110
4	7.0	16	112	2	56
5	6.0	150	900	5	180
7	4.0	130	520	5	104
8	-4.25	180	765	6	127.5
9	-7.0	15	105	2	52.5
1,6,10	Output Return	-	-	-	-
TOTAL	-	-	$\approx$ 3.2k	27	-

effects due to aging or radiation damage during the lifetime of the experiment. The main electrical specifications of the LVPS are summarized in table 7 [32].

The LVPS mechanical form factor is shown in figure 26. The unit fits in a rectangular steel chassis with a protruding "nose" where the output connections are located. On each side of the chassis four nylon "buttons" at the corners prevent electrical contact between the chassis itself and the Tilecal on which it is mounted, in order to maintain electrical isolation between the detector subsystems. Each LVPS unit is installed near its corresponding FEC, mounted on the Tilecal structure. Two thick G10 rails are anchored on the Tilecal fingers. Two iron covers on the front and top side of the LVPS have been installed to shield the ATLAS static magnetic field, preventing possible saturation of the magnetics in the LVPS module circuitry. Figure 27 is a picture of the LVPS and

Table 7. Main electrical specifications of the LVPS.

Parameter	Value	Unit	Condition
Line Regulation	$\pm$0.5	%	Low to high line
Voltage set point	$\pm$0.1	V	within values from table 6
Load Regulation	$\pm$ 10	%	no load to full load
Temperature Coeff.	<0.05	%/^{o}C	over operating temperature range (0-75^{o}C)
Voltage Ripple	10	mV	measured on the power bus with CMB installed
Efficiency	>75	%	measured at the nominal load
Max. Magnetic Field	70	G	measured inside the LVPS chassis

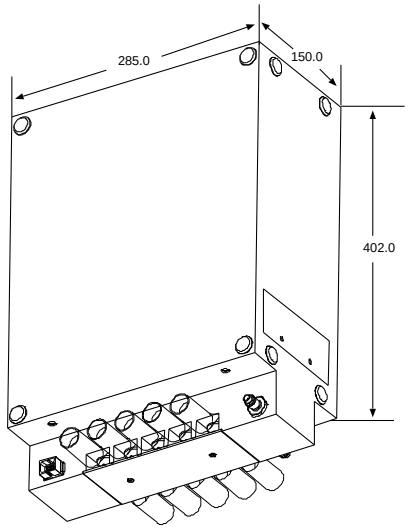

Figure 26. Drawing of the mechanical outline of the LVPS, with the main dimensions shown (in mm).

FEC installation on the EMB during commissioning.

Immunity to magnetic fields has been verified with single modules tested in a magnetic field generated by a large dipole. Output voltage, ripple, efficiency and switching frequency, were verified to stay reasonable for a magnetic field of $\approx$ 100 Gauss in the worst case orientation, well above the specification of 70 Gauss. For even higher fields, the main power transformer in the converter would saturate excessively.

The LVPS was qualified for radiation tolerance. In addition to total ionizing dose and neutron fluence effects, a particular concern was destruction of a module due to possible Single Event Burnout (SEB) of the power MOSFET. SEB cross-sections on single MOSFET devices were measured through a non-destructive technique described in MIL-STD-750D Notice 3 Method 1080. No SEB events were measured at the nominal input voltage. Linear extrapolation to 300 V yields an estimated cross-section of 5×10^{-17} cm^{-2}. This value corresponds to a probability of less than 5% that one or more SEB events will occur in 10 years among all the LVPS installed on the detector.

With 75% efficiency, the heat dissipation of the LVPS at full load is $\approx$800 W. The 27 modules are mounted on a thick aluminum heat sink with water channels distributed over the surfaces to optimize the heat exchange to the hot spots of the modules. The inlet and outlet water connec-

Figure 27. Photograph of a LVPS and FEC installed on the ATLAS detector and being commissioned. The LVPS is the white box visible toward the bottom of the photograph, while the FEC is visible above the LVPS.

tions are located on the LVPS nose where quick disconnects provide the connections to the water distribution circuit.

The output voltages are monitored in the FEC as described in section 5.8. However the LVPS internally monitors output voltages on each individual module and feeds them to a local control board to verify that the functionality of each module is within the specification requirements. In addition the LVPS provides externally several diagnostic signals, including "All modules good", a logic signal that is high if all 27 modules are working properly and which turns low if any module is malfunctioning. The "All voltages good" signal uses the same logic except that a condition is flagged only if two or more modules of a voltage rail have failed. There is also an overtemperature shutdown signal which monitors the temperature of a thermistor mounted on the internal LVPS cooling plate. If this temperature rises above 60° C, logic circuitry on the control board raises high this output indicator. Finally, a "temperature over-ride" control signal is provided that can over-ride the shutdown logic for over-temperature. It has to be tied to the 280 V return to be activated.

6.3 HEC low voltage system

The HEC LV System has to provide the low voltage power for the Preamplifier and Summing Boards (PSBs) mounted on the HEC detector in the cryostat (details of the HEC cryogenic electronics are presented in reference [33]). Each HEC endcap houses a total of 160 PSBs.

The HEC LV system begins with the ATLAS three-phase 400 VAC network, which is converted to 300 VDC by a 4.8 kW power supply located in USA15. The 300 VDC output is dis-

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Table 8. List of HV modules used for the various parts of the LAr calorimeter system.

Detector	Operating Voltage (V)	Maximum Current (μA)	Number of 32-Channel Modules
EMB	2000	75	53
EMEC	1000 to 2500	200	56
HEC	1800	75	32
FCAL	250,375,500	6000	14
3×10 purity detectors	2500	75	2

tributed to eight LV boxes on the cryostat, each of which provides power to 40 PSBs. The LV box uses DC-to-DC converters to produce three intermediate voltages (9 V, 5 V and -3 V). Two DC-to-DC Converters are used for each output voltage, with their outputs coupled via diodes.

The LV box outputs are routed to LV Distribution Boards mounted in the HEC FECs. On the Distribution Board, low dropout voltage regulators are used to provide the final three supply voltages (7.2 V, 3.2 V and -1.6 V) for the PSBs. The voltages and currents are measured, and can be individually switched on or off.

The HEC LV system is controlled via the CANbus. Each 300 VDC PS is controlled and monitored. Each LV box contains an ELMB board and measures a total of 1920 PSB voltages and currents. In addition, 28 internal voltages and currents are monitored. A backup serial protocol is present in case the ELMB is damaged due to radiation.

7. High voltage power supplies and distribution

The HVPS system provides the drift voltage across the LAr gaps in the calorimeters between electrodes and absorbers. The LAr calorimeter cells are connected in about 4700 HV supply groups, distributed roughly equally among each of the three cryostats. Each HV group is connected via a cryostat HV feedthrough port to a single HV channel in the calorimeter. For illustration, the layout of a HEC HV channel is shown in figure 28.

A summary of the HV module count with channel parameters is listed in table 8. A total of 157 commercial 32-channel HVPS modules [34] are used, mounted eight to a subrack in 20 subracks. The total HV system occupies five racks in USA15. During integration in ATLAS, problems with the HVPS were encountered due to component failures and other issues. These were finally resolved, requiring several modifications at the board and component level (more details can be found in reference [35]). As an example, the specifications of a 200 μA HV module are summarized in table 9.

In order to avoid stresses to the LAr detectors caused by loss of HV, the HV system is powered via an Uninterruptible Power Supply system. Each rack has closed-circuit air-cooling with water-cooled heat exchangers similar to the LVPS racks, as described in section 6. In case of loss of the primary cooling water, the cooling system switches automatically to an alternative non-recycling water circulation system.

Each HV channel is individually controlled (on/off, voltage, trip current, voltage ramp speed) by software. For additional protection, per-module voltage and current limits are selectable in

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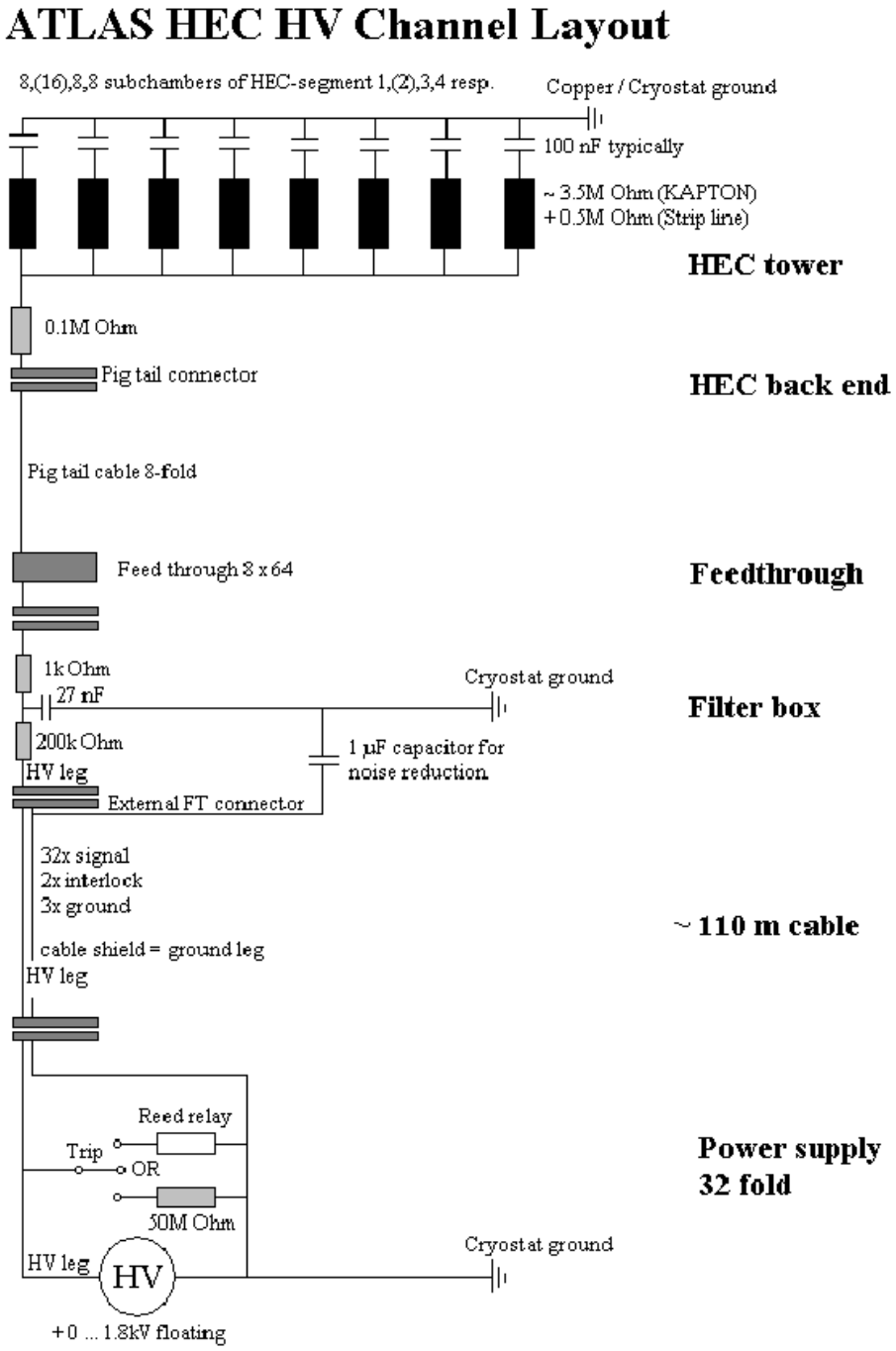

Figure 28. Schematic layout for one HV channel connected to the HEC calorimeter.

hardware. The control and monitoring of the subracks and modules uses the CANbus. The software sets the requested values of the voltages and current limits and, in continuous communication with the modules, monitors and logs the actual voltage, current and channel status. Each subrack and module is equipped with hardware interlock connections which will ramp down the HV in case of an alarm condition (such as cable disconnection or a cryogenics failure). The modules

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Table 9. Specifications for a 200μA HV module.

Parameter	EDS 20 025p-204-KB3
Channel density	32-channels in 6U Euro cassette (40,64 mm $\times$ 220 mm)
Output current I_O	max. 200 μA
per channel at V_O	+ 2550 V
Ripple and noise (f = 10-100 MHz)	< 20 mV (at max. load)
Current limit $I_{\max}$	Potentiometer ($I_{\max}$ same for 32 channels)
Voltage limit Vmax	Potentiometer ($V_{\max}$ same for 32 channels)
Interface	CANbus interface
Data format (setting, measurement)	floating-point single precision
Voltage measurement	resolution better than 50 mV
Current measurement	resolution better than 4 nA
Accuracy of voltage measurement	$\pm(0.01\% \times V_O + 0.02\% \times V_{Onom})$ for one year
Accuracy of current measurement	$\pm(0.1\% \times I_O + 0.4\% \times I_{Onom})$ for one year
Temperature coefficient	$<5 \times 10^{-5}/K$
Stability	$<5 \times 10^{-5}$ (no load/load and $\Delta V_{\rm IN}$)
Rate of change of $V_{\rm OUT}$ via software	Up to 500 V/s
Power requirements $V_{\rm IN}$	+ 24 V (2.0 A) and + 5 V (0.4 A)

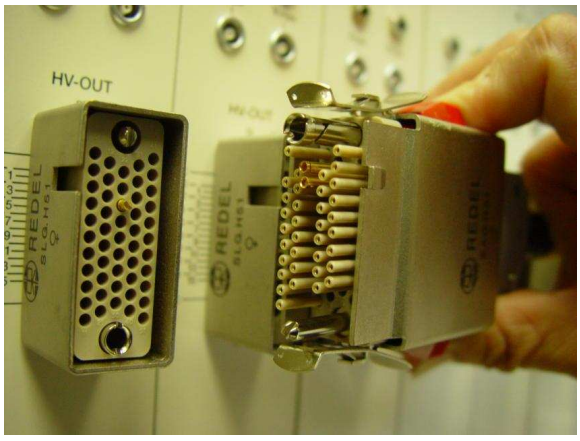

Figure 29. A HV module output and a multi-conductor cable connector as used for the EMB.

are equipped with a crowbar relay which, if operated, discharges the detector capacitance within seconds rather than many minutes. The relay functionality can be programmed by software and is normally disabled.

Shielded 37-conductor HV cables, rated for 3 kV and tested to 6 kV, bring HV from USA15 to the detector. The cables have a 13 mm outer diameter and are typically 120 m long. They are terminated by 51-pin multi-contact HV connectors like the one shown in figure 29.

At the detector, the HV cables are connected to HV Filter modules mounted on the HV Feedthroughs of the LAr Cryostats [36]. RC filters in these modules reduce potential electrical

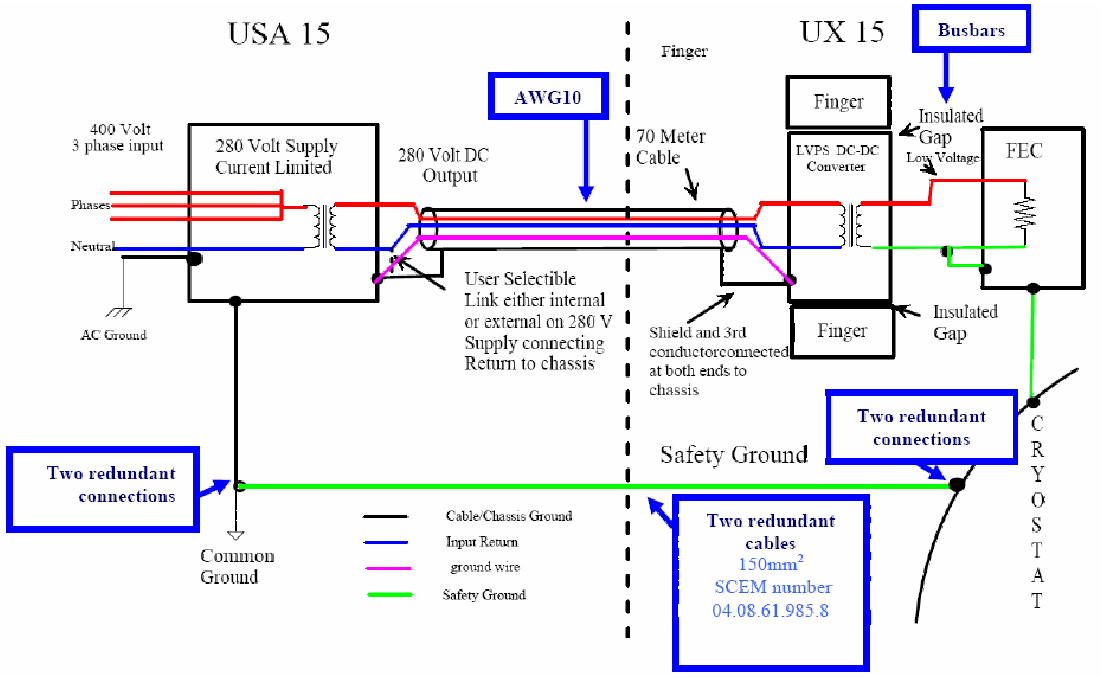

Figure 30. Grounding scheme for the LV system.

pick-up noise entering on the HV lines. Each 3U $\times$ 10HP filter module contains 64 RC filters, divided over four daughterboards, with typical component values R=200 kΩ and C=27 nF (5 kV). Individual filter sections are well separated electrically to prevent leakage, corona, and discharges. The ground wires and cable shields of the HV cables are interrupted at the entrance of the filters in order to avoid ground loops (see next section). The HV current returns to the HV modules via the safety ground links of the corresponding cryostat.

8. Grounding scheme

Great care has been taken to ensure electrical separation and controlled grounding between the different ATLAS subsystems [37]. In addition, it is very important to control the electrical connections between the detector and USA15, as multiple conducting paths introduce the possibility of ground loops, which can cause unwanted additional sources of noise and baseline shifts.

Grounding and isolation of the control and monitoring system implemented via the ELMBs was discussed in section 5.8. The LV grounding scheme is shown in figure 30. The 280 V return and the cable shield are connected together at the USA15 racks to the USA15 ground. However, they are not connected to the output current return of the DC-DC converters, which are connected to the LVPS chassis (for safety) and ultimately to the FEC enclosure and to the cryostat. The DC-DC converters inside the LVPS on the detector provide DC-isolation to the cryostat ground.

Figure 31 shows the grounding scheme of the HV system with all relevant connections between the HV module, HV filters, and cryostat. The HV source is electrically floating relative to cavern ground and is only referenced to the cryostat's potential. For electrical safety, each subrack

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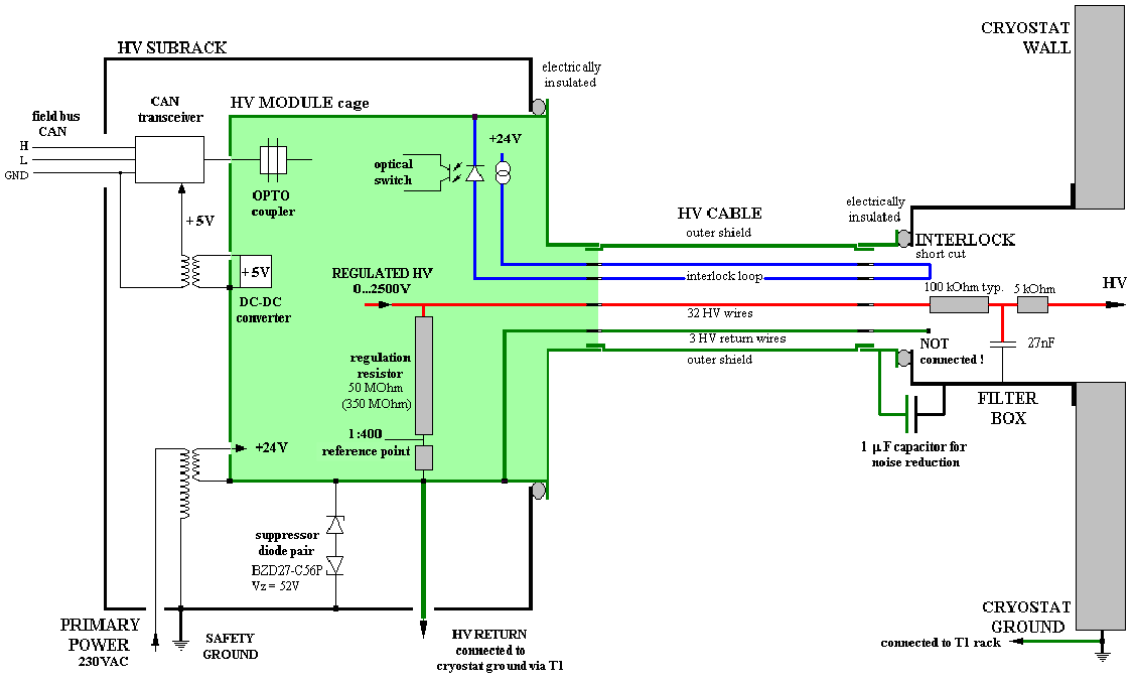

Figure 31. Grounding scheme for the HV system.

is equipped with a back-to-back diode pair connecting the HV reference ground and the general rack ground.

The shields of the HV cables are connected on the side of the USA15 ground but were originally disconnected at the cryostat end. However, during detector commissioning tests in the ATLAS cavern, large high frequency noise signals were observed in the readout, especially the presampler channels. The source of the noise was established as an AC potential difference between the USA15 ground and the cryostat ground, which would enter the cryostats by coupling to the HV cables. To solve this problem, a 1 μF capacitor was installed between the shield of the HV cables (USA15 ground) and the HV filter ground (cryostat ground). This modification was implemented inside the HV filter boxes, and cured the noise problem.

The connections of the trigger cables, the only LAr analog signals between the detector and USA15, and their shields are also carried out with attention to detail. The basic principle is to extend the Faraday cage of the calorimeter to the far end of the cables in USA15, but not to make a DC connection at USA15. Instead, we leave the possibility to connect the shield to the analog ground on the Receiver through a capacitor, permitting noise which is common to both the signal and ground to be reduced if necessary. The signal itself is passed through a transformer whose center tap at the input is connected to the Receiver analog ground. AC-coupling is possible in this system without the undesirable effects of rate-depedendent baseline shifts as the LAr signals are bipolar with area balance. (Baseline shifts are expected for the Tilecal signals, which are unipolar, but given their amplitude distribution and expected rates, their effect is expected to be negligible.) The common terminal of the Receiver power supplies is connected to the crate ground, which is in turn connected to the ground line running between USA15 and the cryostats.

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The output signals from the Receiver are also transformer-coupled, and they are sent over twisted-pair cables which are identical to the input cables. The shields are handled in a similar way as the shields on the input cables, and the only DC connection is made at the receiving (preprocessor) end. The purpose of this arrangement is not so much to prevent ground loops but to reduce the effects of digital noise generated in the preprocessor modules on the Receiver signals.

During installation and cabling of the calorimeters in the ATLAS cavern, a ground short detection mechanism (incorporating an audible alarm) has been operating on each cryostat to quickly identify and remove any accidental ground connections.

In summary, all LAr services and connections to the cryostats are electrically isolated. The single DC current return path (in particular for the HV return current) is a single connection (composed of two cables for redundancy) linking the cryostats to a single grounding point in the USA15 counting room close to the L1 trigger racks. This configuration avoids parasitic ground loops.

9. Cable plant

The cabling of the ATLAS detector has been a major task with substantial manpower and many teams involved in planning and execution. For the LAr system there are many long cables connecting the FE and BE electronics. Their unit of repetition is one FEC. For each FEC the connections include typically one 280 VDC power cable, four copper trigger cables, one optical fiber cable bundle containing 48 individual fiber connections for digital signal data transmission, and one optical fiber bundle with six individual fibers for the TTC signals. Additionally, other services arrive at a FEC from different points in the ATLAS underground cavern and USA15. These include temperature probes and anti-condensation heaters on the feedthroughs, cryostat and calorimeter temperature probes, and LAr purity probes inside the LAr volume.

Cables and services enter the ATLAS cavern from USA15 via the cable galleries and typically follow one of several routes. These include a outer ring and inner ring routes for the barrel (see figure 32). The inner ring has the shortest path and is used for time-critical cables, including the trigger and TTC cables. From the middle ($z = 0$) of the cylindrical Tilecal at the correct azimuth, the cables are routed in horizontal cable trays toward the end faces to the spaces in between the fingers of the Tilecal. From there radially inwards they reach the FEC.

For the endcap calorimeters, cable chains located in three azimuthal sectors are used to route the connections. The use of chains allows the endcap calorimeter to be retracted for access reasons without disconnecting the various services, including cables and also cryogenics connections.

10. Summary

We have discussed the system architecture, design and implementation of the FE electronics developed for the readout of the ATLAS LAr calorimeters. The overall system performance has been verified in dedicated tests before launching production, and has been shown to meet or exceed the demanding specifications. The various boards and other components of the system have been extensively tested and qualified during production. Commissioning of the entire system is currently underway in the ATLAS cavern, in anticipation of the approaching turn-on of the LHC.

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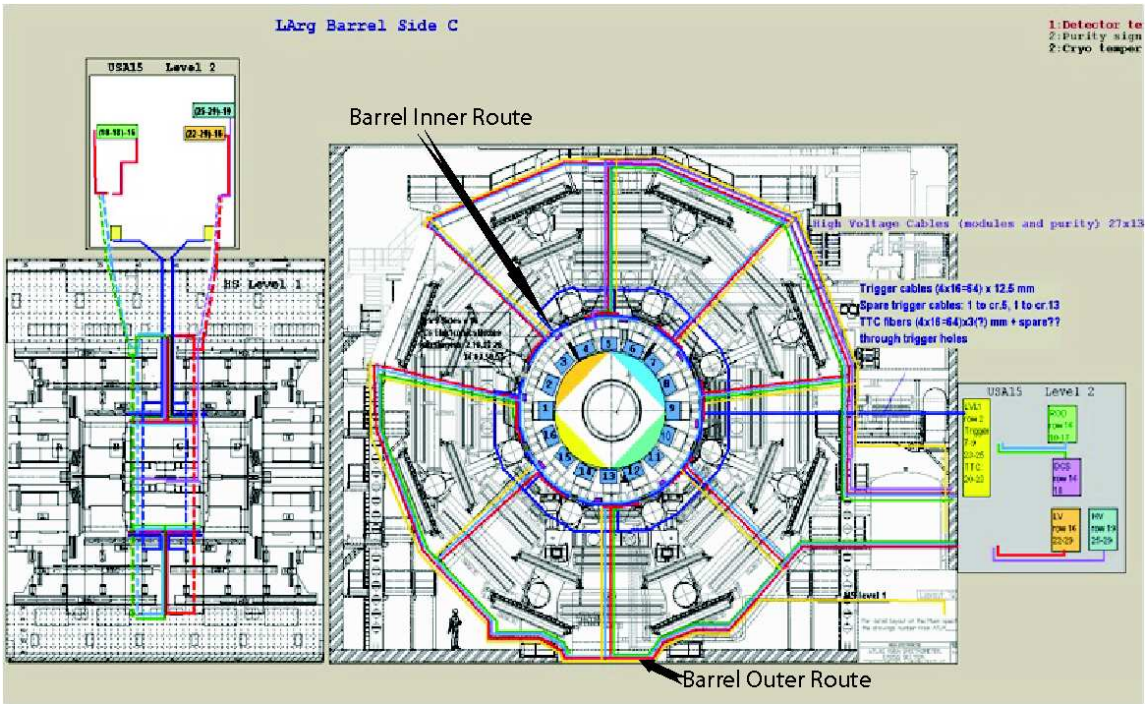

Figure 32. Cable routing around the LAr barrel calorimeter.

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A. The SPAC serial control system

The SPAC protocol requires a minumum of two unidirectional lines: one Master-to-Slave line (MS), and one Slave-to-Master line (SM). Each is duplicated for reliability purposes. These are

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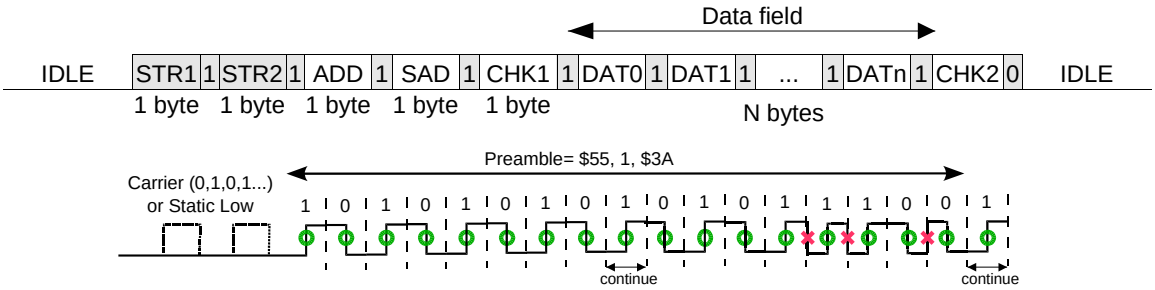

Figure 33. (Upper) Sketch of a typical SPAC frame, made of 9-bit data words. (Lower) Predefined preamble indicating the start of a frame (denoted STR in the upper figure).

transmitted on separate unidirectional optical links between SPAC Masters in USA15 and Controllers in FECs. For each direction, data and clock are combined to form a single signal in the same way as in the Manchester coding system: a logical one (zero) is coded by a low-to-high (high-to-low) transition.

The protocol enables point-to-point read or write data accesses or broadcast write data accesses to all or some of the slaves of a network, at a raw data bit rate of 10 Mbps. Each serial slave in the network is identified by a unique 7-bit address. One of these addresses is reserved for global broadcast accesses, and 15 others are reserved for local broadcast accesses. Each serial slave is also assigned a 4-bit local broadcast address that determines which local broadcast command it should consider.

Any SPAC frame (figure 33) is a sequence of 9-bit data words, as sketched in the upper figure in figure 33. The 9-bit data word consists of one byte of useful data, sent in big endian order (least significant bit first), and a Continue/Last bit, which is a logical one for all words except the last one, where it is a logical zero. When no frame is being transmitterd, the corresponding serial line is in an idle state, indicated either by a static low level or a sequence of indefinite length of logical `{0,1}` doublets that form a carrier signal.

The start (STR) of a frame is indicated by a preamble, made of a two-byte pre-defined sequence of logical zeros and ones ($55, a Continue bit, $3A, and another Continue bit, forming the pattern shown in the lower figure of figure 33).

The fifth word is a ”partial” checksum (CHK1), calculated on the slave address and the sub-address fields of the frame. If a slave detects a checksum error at this level, it ignores the subsequent data bytes of the frame in order to avoid writing data to the incorrect register on a FE board. The last word is the data checksum (CHK2), calculated only on the data field if it exists (bytes after the partial checksum). When a slave detects an error in an incoming frame, it can generate an interrupt frame, defined by assertion of a static high level lasting approximately one microsecond. At the end of the frame transmission, the lines goes back to its idle state (static low or carrier signal).

The same basic format is used for both MS and SM communications. Frames produced by the Master (Slave) are indicated by the direction bit of their second word being set to one (zero). The words between the fifth (partial checksum) word and the last (data checksum) word comprise the data field. Its function varies according to the context:

Figure 34. Photograph of a CMB. The output connector to the ELMB is visible in the upper left.

- In a write frame produced by a Master, it contains the data bytes to write to the Slave.
- In a read request frame produced by the Master, it indicates the number of data bytes to read from the target Slave (or byte count). In this configuration, the data field cannot contain more than two bytes, and if it is empty, the byte count is assumed to be 1.
- In an answer frame produced by a Slave in response to a read request from the Master, the data field contains the data read from the Slave.

B. Implementation of the Front End Crate Monitoring System

As mentioned briefly in section 5.8, the FECMS monitors the FEC voltages and the water temperatures of both the FECs and the LVPS units, and controls the LVPS ON/OFF state through the 280 V supplies.

The ELMBs access the FEC voltages via the CMB, a simple PCB installed in the FEC. There is one CMB installed in each of the 58 FECs. Since no connection to the baseplane is required, the CMB is not a full-sized FE board, but instead had overall dimensions 490 mm $\times$ 203.2 mm (a photograph of a CMB is shown in figure 34). The voltages from the FEC power bussbar are connected to the CMB through a standard power comb. The CMB provides filtering of the FEC power, via 500 μF ceramic capacitors mounted on each of the seven voltage lines. In addition, the CMB provides attenuated (202:1) copies of the voltages on an additional connector which is connected to the ELMB. Also, as described below, while digital power to the ELMB is supplied by the CANbus PS in USA15, the CMB uses the +11 V line from the FEC to power the analog section of the ELMB. In several FECs the CMB are used to mechanically support small PCBs housing radiation monitoring sensors. The sensor output cables are routed from the CMB to another system of dedicated ELMBs positioned at the base of the calorimeters.

For LAr, the ELMB has been adapted through the use of a customized adapter board. Figure 35 shows the three PCBs sandwiched together to form the ELMB sub-assembly: the ELMB itself, the ELMB motherboard, and the adapter board. The ELMB digitizes the incoming analog signals and monitors the status of the I/O digital ports. The ELMB motherboard houses also different plug-in

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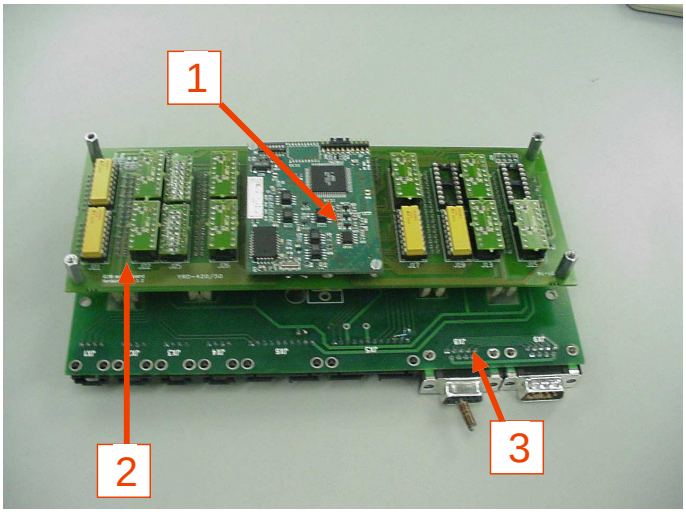

Figure 35. A view of the ELMB sub-assembly, which consists of the ELMB [1], Motherboard [2] and the Adapter Board [3].

boards connected to the ADC inputs. These plug-ins allow customization of which sensor to read and monitor (e.g. voltages, thermocouples, platinum resistors, etc.). Unused ADC channels are terminated with resistive arrays to prevent noise pick-up.

The ELMB module provides electrical isolation between the CANbus, the digital and the analog sections of the board (see reference [29]). Each section can be powered independently if desired. Given the grounding configuration of the LAr detector, as described previously, we adopted a configuration where the CANbus and digital sections of the ELMB module are powered from the CANbus PS installed in USA15. A local balun filter provides a low-pass filter (-40 dB at 1 MHz). Analog power to the ELMB is provided by the +11 V supply on the FEC through the CMB. A failure of the +11 V supply at the level of the FEC will shut down the analog section of the ELMB, preventing the system from monitoring the FEC and triggering a software interlock to disable the corresponding 280 V PS.

Since the ELMB monitors signals referenced to both the cryostat ground and to the USA15 side of the crate PS, proper isolation methods must be used to avoid ground loops. Both high resistance and optical isolation techniques are employed. PT-100 probes are measured using a four-wire differential measurement, eliminating resistive losses in the wires and providing isolation. The probe itself is not in ohmic contact with any other part of the system. FEC voltages are measured using a single-ended resistive divider adapter card. The measurement uses series resistors at each ADC differential input to provide isolation. The LVPS Control and Monitor are connected to the digital I/O ports of the ELMB using optocouplers. The ELMB sub-assembly is attached to a metal sleigh, which in turn attaches to the ELMB cover via two captive front-panel screws. All connections are made on the front panel except for those special modules that have to connect to the CANbus cables from USA15. On the detector each ELMB assembly is mounted into a shielded metal box mounted on the Tilecal fingers.

The ELMBs on a face of the cryostats are daisy chained together through CANbus cables to form four partitions on the detector and correspondingly four partitions in USA15 where the 280 V

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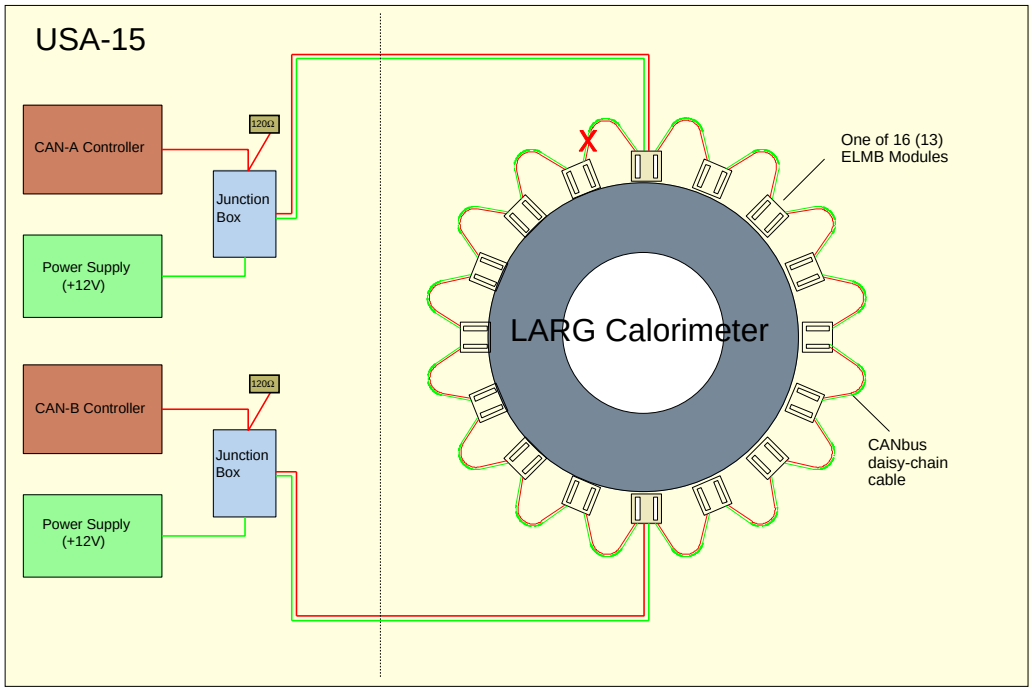

Figure 36. Loop configuration for the ELMB nodes in a partition on the detector.

power supplies are installed. The ELMBs are connected in a loop configuration which provides the best protection for the loss of cable connection or the interruption of a cable itself. Two long (70-100 m) cables connect to the loop in opposite positions on the detector side and to the CANbus interface controllers in the USA15 side (see figure 36). Normally only a single controller is enabled and drives the CANbus. The second controller provides the cable termination and is used as a backup. Signal integrity is preserved, since the loop length is short compared to the total length of the transmission lines and the CANbus signals are driven at a maximum frequency of 100 kHz.

A computer located in USA15 acts as the local DCS server for the FECMS. It accesses and sets the state and the configuration of each of the 58 FECs. The FECMS server is integrated in the overall ATLAS DCS system and functions as one of the detector's state machines. Implemented in this software are the oversight functions for cooling water temperature and voltages on the FECs which will shutoff the corresponding 280 V supply should any of these values go out of the pre-defined acceptable ranges.

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C. Photographs of components of the Front End Crate infrastructure

Figure 37. Photograph of a warm cable used to connect the calorimeter signals from the feedthrough pin carriers to the FEB inputs via the baseplane.

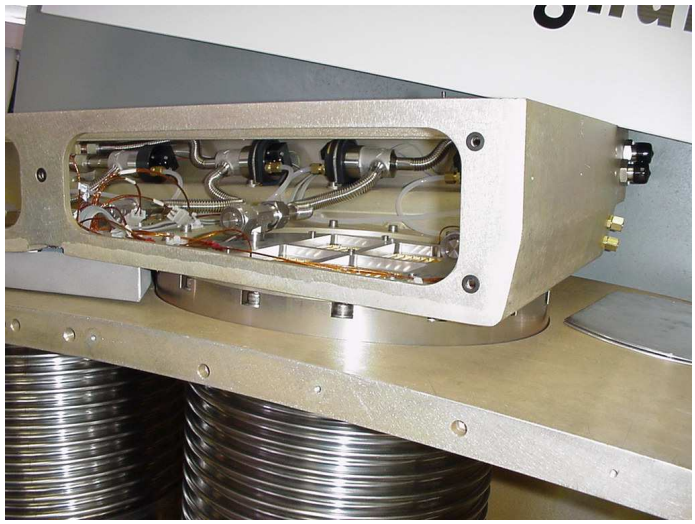

Figure 38. Photograph of a pedestal installed on a detector mockup, with no warm cables installed. The vacuum lines and pneumatic valves are visible inside the pedestal.

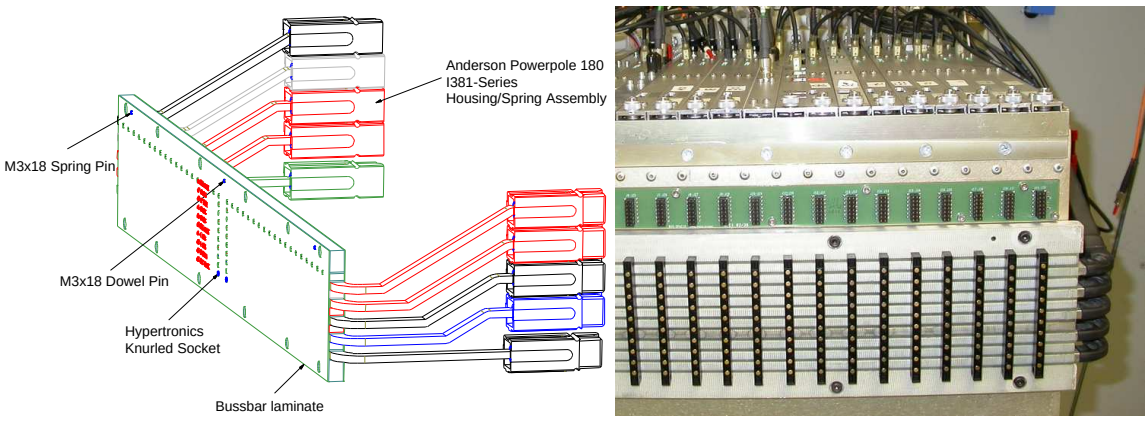

Figure 39. Assembly drawing (left) of a power bussbar and photograph (right) of a bussbar installed on a FEC. The (black) power combs can be seen inserted through the bussbar. The (green) SPAC bus can also be seen, mounted above the power bussbar.

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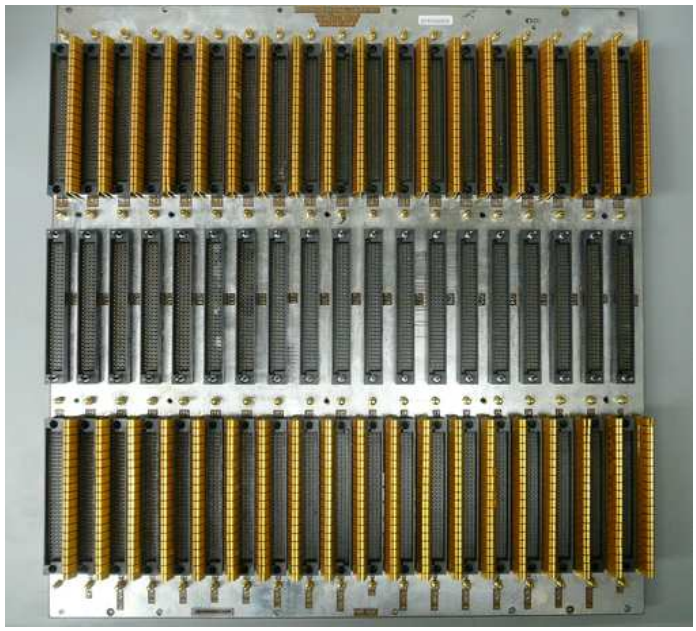

Figure 40. Photograph of a FEC baseplane for the EMB. The upper and lower rows of connectors are used for input signal connections to the FEBs, and are surrounded by custom springs for improved grounding. The middle row is used for connecting the L1 sums from the FEBs to the TBB/TDB.

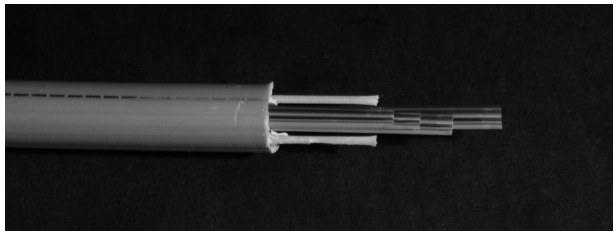

Figure 41. Photograph of an optical cable used for transmitting FEB digital readout data from the FEC to the BE electronics. The fiber ribbons are visible emerging from the outer protective sheath.

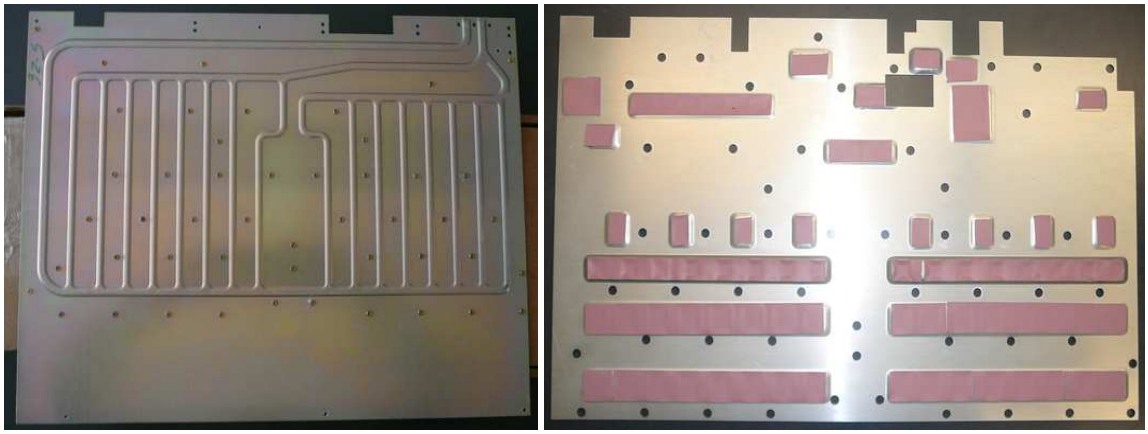

Figure 42. Photographs of (left) a cooling plate and (right) a heat transfer plate with thermal pads applied, ready for installation on an FEB.

Figure 43. Photograph showing racks in USA15 housing the 280 V power supplies.

D. Acronyms used in the paper

ADC - Analog-to-digital converter

ASIC - Application specific integrated circuit

BE - Back end electronics

BNL - Brookhaven National Laboratory

CALIB - Calibration board

CANbus - Controller-area network bus

CMB - Crate monitor board

CONT - Controller board

DAC - Digital-to-analog converter

DCS - Detector control system

DCU - Detector control unit chip for measuring voltages and temperatures

DMILL - Name of radiation hard semiconductor process used for some of the custom ASICs

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DSM - Deep submicron (referring to 0.25 μm radiation-tolerant semiconductor process)

DSP - Digital signal processor

EC - Endcap

ELMB - Embedded local monitoring board

EM - Electromagnetic

EMB - Electromagnetic barrel calorimeter

EMEC - Electromagnetic endcap calorimeter

E_T - Transverse energy

FCAL - Forward calorimeter

FE - Front end electronics

FEB - Front end board

FEC - Front end crate

FECMS - Front end crate monitoring system

HEC - Hadronic endcap calorimeter

HFEC - Half front end crate

HFFR - Halogen-free, flame-retardant

HVPS - High voltage power supply

I2C - Inter-integrated circuit

L1 - Level 1 trigger

L1CAL - Level 1 calorimeter trigger

LAr - Liquid argon

LHC - Large hadron collider

LSB - Layer sum board

LVPS - Low voltage power supply

MS - Master-to-slave

Opamp - Operational amplifier

PCB - Printed circuit board

PECL - Positive emitter-coupled logic

PLC - Programmable logic controller

PS - Power supply

PSB - Preamplifier summing board of the HEC

ROD - Readout driver board

SCA - Switched-capacitor array analog memory

SCDB - Serial control daughterboard of the L1 Receiver

SEB - Single event burnout

SM - Slave-to-Master

SMC - Surface-mount component

SPAC - Serial Protocol for ATLAS Calorimeters (serial control system)

TBB - Tower builder board (for the L1 trigger sums of the EM calorimeters)

TDB - Tower driver board (for the L1 trigger sums of the HEC and FCAL)

Tilecal - Scintillator-tile-based hadronic calorimeter

TTC - Trigger, timing and control system

TTCrx - TTC receiver chip

USA15 - Underground service area 15 (off-detector underground counting house)

USB - Universal serial bus

VGA - Variable gain amplifier

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