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BEPC COMPUTER CONTROL SYSTEM

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Abstract This paper describes the development and construction of the computer control system for the 2.2-2.8 Gev Beijing Electron Positron Collider (BEPC) during 1985 to 1988. A Vax-Vcc-Camac system architecture was adopted. Serial optic fiberlink ;extended signal database;dual speed dual accuracy power supply Ramp;on/off and start/stop operation of P.S. system etc. are developed for this system.This system is put into operation and operated normal -ly since end of 1987.

INTRODUCTION

Due to there was a strong desire to provide a working control system at the end of 1987, so the criterion of choice mainly depend upon the time schedule. After discussion with all side finally we decided to adopt the New SLAC SPEAR portable database driven control system architecture, it is the most easy way to establish within three years and can satisfy our BEPC time requirement even this architecture is old. Also we decided to adopt the KEK-AR timing system as BEPC timing system. Under the helps of SLAC and KEK we have constructed this control system and put into operation successfully just in time.

The BEPC machine is composed of three main parts:a 1.4 Gev Linac in -jector;a 1.4 Gev e+ and e- transport line;a 2.2-2.8 Gev storage ring. The equipments and signals to be controlled are summarized into following table:

	Equipment						Signal							
Location	PS	VAC	RF	BM	other	Total	DM	DC	DI	DO	AM	AC	DV	total
Linac	100	95	16	62	10	283	1193	326	0	0	383	141	0	2043
Transp. line	74	32	0	62	44	212	393	263	25	28	113	74	0	896
storage ring	108	146	10	70	51	385	974	458	170	107	296	103	26	2134
Total	282	273	26	194	105	880	2560	1047	195	135	792	318	26	5073

SYSTEM ARCHITECTURE

China is a developing country and BEPC is the first high energy accele-rator.So lacks of experience,limited investment and required short construction period decide our control design criterion are:adopt well-established and cheap technique;arrange system as simple as possible; emphasis the reliability of system;reduce the EMI as more as possible; clearness the boundary of control level in order to easily manage.

The basic system architecture of BEPC is shown in Fig 1. VAX 11/750 and VCC are selected due to low cost and directly using of SPEAR software. VCC is a intelligent Unibus to Camac interface convertor. This programmable channel couples VAX to two system crates, each of which houses several serial branch driver(SBD),each SBD can directly control up to seven user camac crates with max. distance more than 500 m via optic-fiber link.BUSY-READY handshake protcol is used in communication link between VCC,SBD and user Camac crate.There are total about 14 optic-fiber link, 30 Camac crates, 300 Camac functional modules used in this system.Devices of BEPC accelerator are distributed in area of LxW =350X80 meter squares.The entire control system are divided into three level: upper level is computer and system crates located in main control room;middle level is the user Camac and interface modules located in local control room; lower level are all of the equipments which are located in the equipment room. In order to reduce the EMI two levels isolation are arranged: first is optic fiber isolation between MCC and local control room;second is using analog or digital optic-isolator IC or relay contact between Camac function modules and equipments.The con-trol system contains three main consoles,architecture of which is ado-pted from SLAC PEP. Each console contains a 512 x 512 color graphic display, a 8 x 8 matrix touch button panel and a general purpose programmable slew knob.

SOFTWARE SYSTEM

Basicly the BEPC system software is presented as a transfer from SLAC SPEAR. Features of all of the signals or parameter are contained in a design file called CALSIG.DAT, which is read by both people and comput-er. Program read it to generate the BEPC database structure,which be-

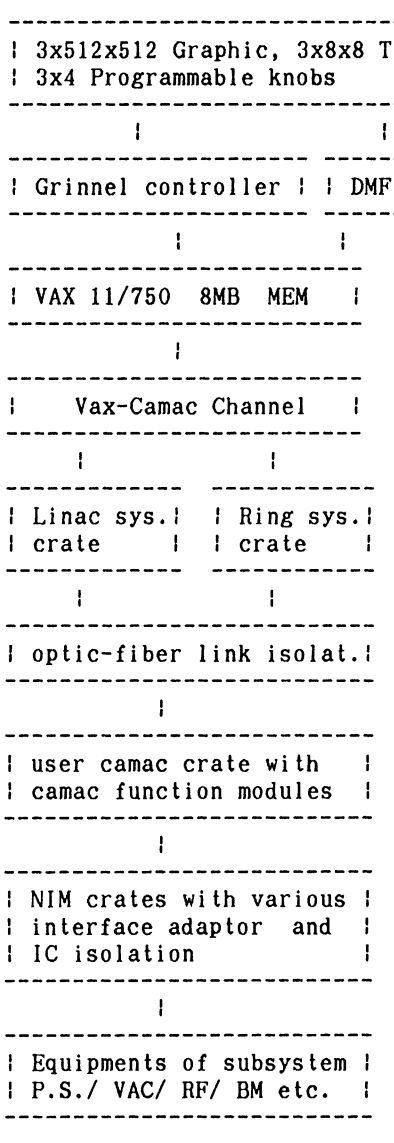

Fig 1. Block diagram of BEPC control sys.

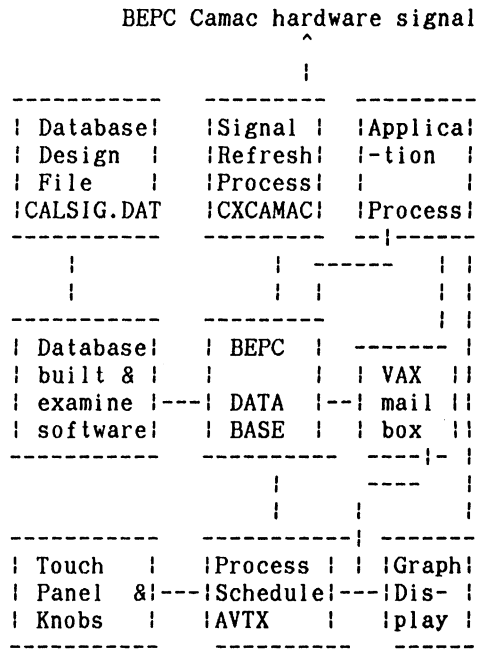

Fig 2. Block diagram of BEPC system

comes the center of communication for all of the software.Hardware sig nal is sent and refreshed to database through database signal refresh software process CXCAMAC.Operator massage and required operation enter -ed from touch button and knob are scheduled by process AVTX, then either transfer to database or communicate to selected application pro -cess or subtask via VAX mailbox, or send required message to CRT dis-

play.The block diagram of the BEPC control software system is shown in Fig 2.

BEPC control software is classified into several level. First is process level,process are scheduled by VMS operating system. each process has several subtasks which are not required parallel operation; second is subtask level, each subtask may be a subroutine, entry or function. Subtask within a same process can't run at the same time and are scheduled by a subtask schedule program inside the process; third are all of the subroutine, entry and function etc. except those defined as subtask .

Database software

The CALSIG.DAT file is the main database design file. In this file the hardware signal are divided into seven signal class as in above table, each signal has a unique signal name, each signal has a 256 bytes leng -th signal description block called SDB. All of the information and attribute of this signal, such as signal unit;display name,Camac CNAF, max. and min. operation value etc. are storaged in this SDB.All of the software can use these complete information of selected signal via this SDB.

Panel file

In BEPC control system,we select a fixed 8 x 8 = 64 matrix touch panel due to extreme stable without drift. Name & function of each button (x ,y) are fully defined by panel file Nxxx.PNL. which are written by FORTH language. When operator touch the selected button (x.y), panel file software can automaticly send the information to selected process or subtask and then perform the required action.

Database refresh process

SPEAR process XCAMAC is used to continuously refresh the DM ,DI ,AM,AC signals into database. The required execution time for refresh once time (i.e the inverse of refresh rate/sec) is directly proportional to the amounts of signals to be refreshed. There are total about 5000 hardware signals in BEPC control system, 2-3 times more than SPEAR .If we directly use SPEAR database refresh software, the resultant refresh rate is too slow. Therefore we have rearranged and divided the AC signal into several kinds, let AC of P.S. are only refreshed during RAMP

operation, and constant at normal.Thus we can still keep the refreshed rate 1-2/sec as original in SPEAR. This modified XCAMAC process is renamed to"CXCAMAC".

On/off and start/stop operation

This software can ensure the following operation condition ; promiss some equipment are controlled in local by manual,others are controlled by central computer; using "MASK" method to mask out these local opera -tion devices and ensure all the central controlled devices are in"cen -tral " and " normal" status before starting; ensure on/off operation, +/- direction of some power supply units (such as steering and corrs.) are operated as last SAVE status after starting; self system diagnostic before system starting;execution can be single step or continuous.

Dual speed dual accuracy PS RAMP

In BEPC max.number of P.S. units for RAMP will be 98 units (26xmain , 64xcorrs, 8 x Qtrim). Using the original single speed SPEAR RAMP software the min. Iperd (AC setting period) are as long as 80 ms,the total ramp time may be as long as near hour.The reason are arised from; tran -sfer speed of serial link is slower than SPEAR parallel link ; power supply unit for RAMP in BEPC two times more than SPEAR; BEPC hardware signal to be refresh two times more than SPEAR. We rewrite and rearrange the VCC pocket and arrange a different ramp speed and accuracy for MAIN and CORRS . Let number of RAMP steps of MAIN is equal to ten times of CORRS ,and Iperd of CORRS is ten times of MAIN. thus reduce the min. Iperd from 80ms to 20 ms. and have a reasonable ramp time for BEPC.

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