ATLAS SCT POWER SUPPLY SYSTEM

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Abstract

The ATLAS SCT (semiconductor tracker) comprises 2112 barrel modules mounted on four concentric barrels of length 1.5m and up to 1m diameter, and 1976 endcap modules supported by a series of 9 wheels at each end of the barrel.

Each module is powered by its own independent, floating low and high voltage power supplies, referenced to ground at the detector shield. Correspondingly, each module has its own distinct cable chain all the way back to the service cavern.

This presentation outlines the structure and specification of the SCT Power Supply System, including the high level control software and operational model.

I. System Requirements

Although the detector modules used in the barrel and endcap regions are geometrically very different, they are electrically very similar. The desire to provide each module with a single reference potential resulted in the adoption of a single, multi-wire, shielded cable to each module [1] and hence in the location of floating, programmable Low Voltage (LV) and High Voltage (HV) power supply channels together in each Power Supply (PS) crate.

Parameter	Voltage [V]			Current [mA]	
	Min.	Typ.	Max.	Typ.	Max.
Vcc	0.0	3.5	5.1	900	1300
Vdd	0.0	3.5	5.1	570	1300
VVCSEL	0.0	4.0	6.6	2	10
VPIN	0.0	6.0	10.2	0.5	2
I source 0	-	-	8.0	0.08	-
I source 1	-	-	8.0	0.08	-
RESET	0	Vdd	Vdd	-	-
SELECT	0	0	Vdd	-	-
HV Bias	0	150	500	~100nA	5

Table 1: SCT Module LV and HV Power Requirements

The power requirements shown in table 1 were derived following a programme of beam and radiation tests of module prototypes and components of the optical readout system. As each module is irradiated the digital current Idd increases, however as the bias and shaper currents of the front end amplifiers are adjusted to compensate for changes in the module's noise performance, the total power drawn from each LV channel is expected to remain roughly constant. A power increase does however come from the silicon micro-strip detectors, as the bias voltage may be increased from its nominal starting value of 150V up to a maximum of 500V, with the bias current increasing up to the maximum permissible value of 5mA.

II. Power Supply Hardware

In the ATLAS pit, the SCT power supply system comprises a total of 22 racks, split equally between the US15 and USA15 service caverns. In addition to standard units such as the turbine, air deflector and heat exchangers, each rack contains two power pack shelves, one Circuit Breaker Box (CBB), four fan trays and four SCT power supply crates.

Each power pack shelf houses two commercial power packs which generate the 48V DC input needed by the LV and HV cards. All four packs are connected to a common bus, power being distributed to the crates through Miniature Circuit Breakers (MCB) housed in the CBB. Only three power packs are needed to power four fully loaded crates: the fourth pack provides redundancy. The CBB also houses a Power Pack Monitor card which utilises an ELMB card [2] running custom firmware to monitor the status of the power packs and fan trays within the rack.

Each power supply crate [3] services up to 48 SCT modules. It houses 6 HV cards, 12 LV cards, one SCT Interlock Card (SIC), one Crate Controller card (CC) and one shorting card (for safety reasons). A mechanical key system is used to ensure that HV cards may only be inserted into HV slots, and the address of each card is set automatically according to its position in the crate. At each LV/HV card, an oscillator block modulates the 48V DC input such that the power input to each channel may be isolated from ground by means of a transformer. Each crate houses a DC-DC converter which provides power at 5V, common to all active cards. In the case of the LV and HV cards, this powers the card controller block only.

The SCTHV card has 8 channels, each with its own ADμC812 processor. An additional processor handles communication between the channels and the crate backplane. Each channel was designed to output a programmable voltage between 0 and 500V, with a programmable current trip which can be set to a maximum level of 5mA. A later modification added a voltage clamp at the output of each channel, to protect against the possibility that the pass transistor may fail in operation. This has reduced the maximum possible voltage output to around 480V.

The SCTLV card has four channels. Each channel comprises two blocks, each with its own ADμC812 processor. An additional processor handles communication between the sub-channels and the crate backplane. The main function of the analogue sub-channel is to provide the analogue power rail Vcc at a programmable voltage between 0 and 10 V (maximum current 1.3A). It also generates two constant current sources to bias NTC thermistors mounted on the detector module. The digital sub-channel provides the digital power rail Vdd at a programmable level between 0 and 10V (max. current 1.3A), pin diode bias VPIN between 0 and 10V (max. current 2mA) and VCSEL[1] laser diode control line VVCSEL between 0 and 6.6V (max. current 10mA). It also drives the digital control lines RESET and SELECT. Current trips or limits are implemented for all voltage outputs with remote sensing being provided for all high current lines. A programmable over temperature trip using the module's NTC thermistors is also provided as part of the LV card firmware.

The crate controller card utilises an ELMB card running custom firmware to provide a link between the power supply channels and the outside world. Controller Area Network (CAN) bus is used for external communications; within the crate a custom 8 bit parallel bus is used. The non-volatile memory of the ELMB is used to store three user defined sets of channel parameters corresponding to operational states of the detector (ON, STANDBY, OFF). The mapping of channels to cooling structures is also made persistent in the ELMB memory such that state transitions for all modules of one cooling loop may be requested with only a single CAN message.

As part of the regular monitoring cycle of the PS channels, two software trips are actioned by the crate controller. There is a programmable temperature trip, which turns off both LV and HV, and a software HV overcurrent trip. Both are set to lower action levels than the trips implemented in channel firmware and are intended to shut a channel down gently. The fast acting channel firmware trips remain in place to respond to sudden temperature or current excursions.

III. Interlocks

Although arguably not part of the power supply system, the SCT Interlock Matrices, located in the SCT DCS rack in each service cavern, form an important part of the detector safety scheme. The inputs to the matrices are digital signals derived by discrimination of signals from thermistors mounted directly on the detector cooling structures. CPLD devices on the matrix cards are programmed to map these signals to the PS channels, such that power may only be applied to modules for which the cooling system is operational. The matrix units have additional inputs to allow direct connection to be made to the ATLAS Detector Safety System (DSS).

One SCT Interlock Card (SIC) is mounted in each PS crate and receives 13 digital signals from the SCT Interlock Matrix. Twelve of these signals are LV/HV enable lines, one for each group of four channels, and the remaining signal is used to enable the output of VCSEL laser bias voltages from all channels of the crate. All SIC inputs are optically isolated to avoid the inadvertent creation of ground loops.

Additional software interlocks are implemented as part of the high level control software, for example to shutdown all modules of one cooling loop if that loop should fail during operation, or to power off the complete system of modules in the event that the main cooling plant should fail.

IV. Power Distribution

The key objectives of the SCT power distribution scheme are to keep voltage drops within acceptable limits, to minimise mass in the detector volume and to do both of the above at reasonable cost. Conventional cables of three different thicknesses are used in combination with power tape technologies for the sections nearest the detector modules.

The thickest conventional cable, designated type IV, runs between the PS racks and the Patch Panel 3 (PP3) racks located in the detector cavern. These cables vary in length from 14 to 75 metres. Each PP3 patch panel incorporates common mode filtering and voltage limiters. The ATLAS SCT readout ASIC, ABCD3TA [4], is not a constant current design. Changes in the chip's configuration can result in sudden changes in the current drawn and hence in the momentary application of excess voltage, possibly resulting in damage. The PP3 circuit is designed to prevent this.

Thinner type III cable runs from PP3 to patch panel 2 (PP2) where it is spliced directly to even thinner type II cable for the run down to patch panel 1 (PP1). The lengths of the type III and II cables are in the range 11 to 23 metres and 6 to 12 metres respectively. From PP1 the connection through to each barrel module is made by low mass aluminium on kapton power tapes. For endcap modules, two types of power tapes are used. Copper on kapton tapes are used between PP1 and an additional patch panel PPF0; from here down to the module a flexible copper on kapton tape is complemented by copper clad aluminium wires used for the high current lines.

All cables were installed to precise tolerances, both in the sections nearest the detector and within the PS and PP3 racks. Dummy PP1 patch panels were made to the same dimensions as the real boards and these were used to locate the cables correctly at the detector end. These panels included simple circuitry to facilitate connectivity tests of the installed cable chain. The 4088 cable chains comprise a total of 20440 connectors or more than 340, 000 active pins: each cable was comprehensively tested upon receipt and at every stage in the installation sequence.

The conversion efficiency of the power packs together with the LV cards under typical loads is around 65%. Losses in the cable distribution system vary according to cable length. The average loss under nominal load is around 38%, with one third of this being lost in the power tape sections. Hence the overall efficiency of the system is around 40%.

V. Early Experiences

Valuable experience had been gained with the SCT PS system before installation in the pit. Production PS hardware and an early version of the control software based on PVSS [5] was used successfully during macroassembly of the

[1] Vertical Cavity Side Emitting Laser

barrels at Oxford, during macroassembly of the endcap disks at Liverpool and NIKHEF, and during further reception and integration testing which took place at CERN. Although interim cabling was used for this work in place of the full cable chain, the hardware setup was otherwise as close as possible to that intended for use in ATLAS.

The core functionality of the control software was already good at this stage, but with important limitations. The system could not be operated with more than 14 PS crates as it was restricted to a single host computer and although channel grouping for control was possible, this was limited to 8 groups, insufficient for any serious attempt to map the modules to cooling structures. Although not needed at the time, the control hierarchy needed to operate the system within the context of ATLAS was also a significant omission.

VI. Mapping Issues

To facilitate the continued operation of the detector in the event of loss of one or more cooling circuits, the modules are placed into control groups according to the physical cooling structures. In the barrel region, one cooling circuit serves four adjacent rows of modules of one barrel, or 48 modules in total. In the endcap region, one cooling circuit serves one quadrant of one disk which, as not all disks have the same number of modules mounted on them, corresponds to between 13 and 33 modules.

It can immediately be seen that the endcap cooling circuits are not well matched to the power supply interlock modularity of 4 channels. Although a system of 88 crates does provide some channels over and above those needed to operate the detector, it is still necessary to maintain a high packing fraction. To this end, each quadrant of each endcap disk may be serviced in part by each of a number of PS crates. The limited number of "spare" channels within the crates has been distributed so as to reduce the number of cases where one interlock group services modules from two different endcap cooling structures, although it has not been possible to eliminate this phenomenon completely.

The barrel cooling circuits are generally well matched to the interlock modularity; however for several circuits it was not possible to bring all 48 cables to the same PS crate. A further complication in the barrel region is that several of the barrel cooling loops cross the cavern boundary. The PVSS control software therefore needs to be able to combine channels into groups across multiple PS crates and also multiple host computers.

VII. Control Hierarchy and Operation

The ATLAS Detector Control System uses the hierarchical controls component [6] of the JCOP framework, also known as the Finite State Machine (FSM) component, to model the structure of sub-detectors, sub-systems and hardware components. The tree comprises Device Units (DU) capable of controlling and monitoring the equipment to which they correspond and Control Units (CU) or Logical Units (LU) within which FSMs are encoded, capable of controlling and summarising the sub tree found beneath them. Commands are sent down the hierarchy from the top and state and status (alarm) information flows back up. Different portions of the tree may be taken into control by different operators, for example the SCT may be operated as a distinct entity apart from the rest of ATLAS for purposes of debugging.

In the system installed in the pit, the SCT PS software is distributed between 9 computers. One computer, the System Control Station (SCS), operates the highest levels of the SCT control hierarchy including functionality such as command distribution. The remaining eight systems are designated as Local Control Stations (LCS): four are needed to operate the barrel power supplies and four more are responsible for operation of the endcap power supplies. Each LCS is directly interfaced to 11 PS crates over CAN bus, and to the other computers by means of the network.

A subset of the FSM control hierarchy for the SCT is shown in figure 1. The SCT is divided into three Trigger Timing and Control (TTC) partitions to match those used by the DAQ: Endcap A, Barrel, and Endcap C. Each partition is further split into four distinct sub-systems: environmental monitoring (ENV), Power Pack Monitoring (PPM), Power Supply (PS) and Read Out Drivers (ROD). Further discussion in this paper will be restricted to the hierarchy of the PS sub-system.

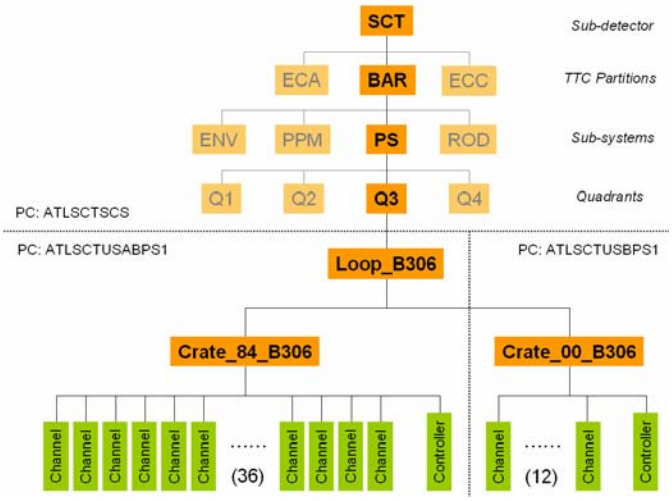

Figure 1: FSM Control Hierarchy for SCT PS Loop B306

The PS subsystem for each TTC partition is divided into four quadrants, numbered Q1 through Q4. Each quadrant contains a number of "loop" control units, one for each cooling circuit of the relevant TTC partition serviced through the corresponding quadrant. Although only one such loop object is shown in figure 1, in the case of the barrel each quadrant comprises 11 cooling loop CUs. Each quadrant of each endcap partition comprises 9 loops, equal to the number of disks at each end of the detector.

Each loop control unit may contain a number of crate group control units and is instantiated on the computer which is directly connected to the majority of channels serving that loop. For example, figure 1 illustrates a loop for which the majority of detector modules are serviced by crate 84, connected to the computer PCATLSCTUSABPS1, with the remaining channels serviced by crate 00 which is connected to computer PCATLSCTUSBPS1. Hence the loop CU is created on PCATLSCTUSABPS1.

Each crate group contains only device units: one DU for each PS channel of the crate which powers a module of the relevant loop and an additional DU corresponding to the crate controller. Whilst it is possible to send a command directly to a single channel using the channel device unit, all multi-channel commands are sent to the crate through the crate controller device unit. This reduces the number of commands which must be sent over the CAN bus as only one message need be sent to request a state transition for all modules of a crate group, thereby improving system performance.

Req. State	LV	HV
OFF	Hardware OFF	Hardware OFF
	Cannot monitor module temperatures	
INITIAL	Software OFF	Software OFF
	Can monitor module temperatures	
STARTING	STANDBY	STANDBY
	Reduced probability of trips at start	
STANDBY	ON	STANDBY
	Used during unstable beam	
ON	ON	ON
	"OK for Physics!"	

Table 2: Operational States of PS Channel Device Unit

A summary of the channel DU states which may be requested is shown in table 2. With the exception of the hardware off state, each requested state represents a combination of the HV and LV control settings stored in the ELMB's non-volatile memory.

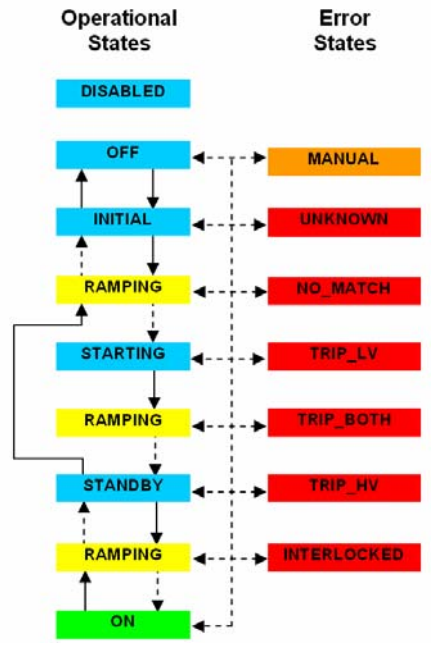

Figure 2: State Diagram for Channel Device Unit

The actual state of each pair of LV and HV sub-channels is periodically evaluated by the crate controller which compares the monitored values against those stored in its memory. This information is returned to the PVSS project as a single byte comprising four bits of LV state information and four bits of HV state information. The channel DU transforms this information into one of the combined channel states shown in figure 2. A number of error conditions are included in the state model, such as the reporting of trips.

The state information must now be propagated back up the hierarchy. The states of all children are combined such that, if any children are in error, the most significant error state is reported. If no children are in error states, the highest state of any child is determined. If all children are in that state, the corresponding complete state is reported. For example, if a crate group has 48 channel children which are all in the ON state, the state of the crate group will be reported as ON. However, if not all children are in the highest state, the corresponding partial state will be reported. For example, if 47 out of 48 channel children are in the ON state, the state of the parent will be reported as ON_PART. In this way, in the event that one channel has failed to respond to a command, this information is propagated up the chain.

It should also be noted that, as the currents drawn by the SCT modules vary according to DAQ activity, all PS channel monitored data is published to DAQ over DDC [7]. It is also possible for the DAQ operator to use DDC to request a number of simple PS actions, such as resetting or power cycling a module. This makes it easier for the DAQ operator to bring the modules into a working state.

VIII. Summary

The ATLAS SCT power supply system comprises 4088 programmable, independent and floating HV and LV channels distributed between 88 crates. The installation of so many cable chains to precise tolerances with full connectivity was a time consuming task, but was managed well. The high level control software, written in PVSS, groups channels together by cooling circuit, then by quadrant. This matches the structure of the cooling system and its controls. Small improvements continue to be introduced into the system; however the core functionality is working extremely well.

The system installed in the pit has been used during commissioning tests of all three TTC partitions, and the SCT PS control hierarchy has been successfully integrated into the central ATLAS DCS. The ATLAS SCT power supply system is essentially ready for physics.

IX. References

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