HARDROC1, Readout chip of the Digital Hadronic Calorimeter of ILC

M. Bouchel, S. Callier, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau

IN2P3/LAL Orsay, France

R. Gaglione, I. Laktineh, H. Mathez

IN2P3/IPNL Lyon, France

V. Boudry, JC. Brient, C. Jauffret

IN2P3/LLR Palaiseau, France

callier@lal.in2p3.fr, taille@lal.in2p3.fr, seguin@lal.in2p3.fr

Abstract

HARDROC is a complete readout chip in SiGe 0.35µm of the RPCs or GEMs foreseen for a Digital HAdronic CALorimeter (DHCAL) at the ILC. The ASIC integrates 64 channels of

- Fast low impedance current preamplifier with 6 bits variable gain (tunable between 0 and 4)
- Variable shaper (75-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC.
- Variable gain fast shaper (15ns) followed by two low offset discriminators to autotrig down to10 fC. The thresholds are loaded by two internal 10 bit-DACs.
- A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

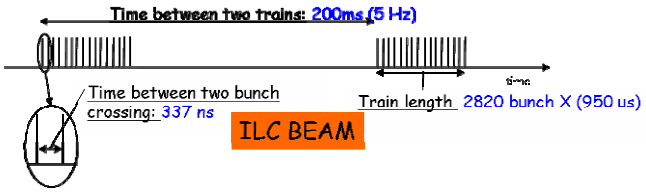
The design and measured performance of the chip will be presented.

I. INTRODUCTION

HARDROC1 (HAdronic Rpc Detector ReadOut Chip) [1] is the first prototype of the very front end chip designed for the readout of the RPC or GEM foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider [2].

The very fine granularity of the ILC hadronic calorimeters ($1cm^2$ pads) implies a huge number of electronics channels ($4\ 10^5\ /m^3$) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption down to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).



HARDROC readout is a semi-digital readout with two thresholds (2 bits readout) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

II. ASIC DESCRIPTION

HARDROC is a 64-channel input very front end circuit. Its main features are:

- AMS SiGe 0.35µm technology (Figure 1)
- $16mm^2$ area
- 3.5V power supply
- 10µW power consumption/channel
- Package: CQFP240

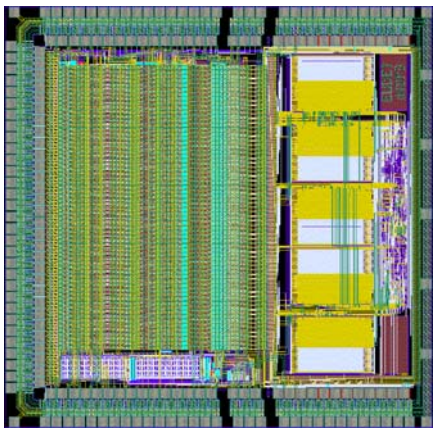


Figure 1: Layout of HARDROC1

The block diagram of the ASIC is given in Fig. 2. Each input signal is first amplified thanks to a variable gain preamplifier which exhibits low noise and low input impedance to minimise crosstalk. It allows accommodating the gain depending of the detector choice, up to a factor 4 to an accuracy of 6% with 6 bits/channel.

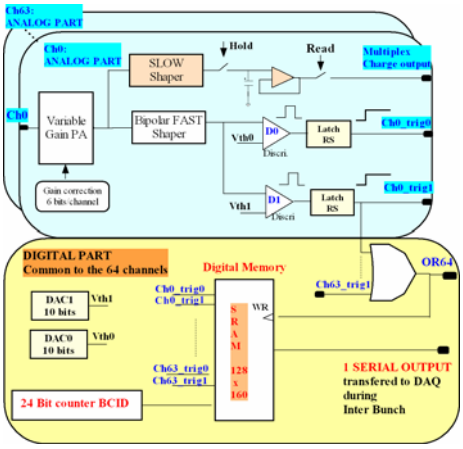


Figure 2: Block diagram of the ASIC

The amplified current then feeds a slow shaper combined with a Sample and Hold buffer to store the charge in 2pF and provide a multiplexed charge output (5MHz) up to 15pC.

In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by 2 low offset discriminators.

The discriminator thresholds are set by two internal 10 bit DACs.

Each trigger output is latched to hold the state of the response until the end of the clock cycle. The trigger1 outputs (corresponding to Vth1 <Vth0) are OR wired to generate an internal trigger used to start the memorization of the 128 trigger outputs as well as the Bunch Crossing Identification delivered by a 24 bit counter, needed to associate hits in the DAQ to bunch crossing ID. It is also possible to capture event data using an external trigger provided from outside the chip.

All the bias currents are programmed through the Slow Control

The chip is power pulsed to decrease the power consumption. 10µW/channel as targeted with a 1% beam duty cycle.

III. ASIC PERFORMANCE

HARDROC has been submitted in September 2006 and received mid December 2006. The performance has been measured using a testboard (Fig. 3) on which packaged or Chip On Board (COB) version can be used. In the COB version, the chip is bonded on the layer 5 of a 6 layers printed board. This version has been studied to estimate the feasibility to embed chips as they will be in the detector.

Figure 3: Testboard with Chip on Board

A. *Variable gain preamp*

The "Super Common Base" configuration of the input preamp allows low input impedance that has been measured to be 50-70 ohms, depending on the (tuneable) current flowing in the preamp. The bias current ibi_pa is small, 5µA, to minimise the power consumption.

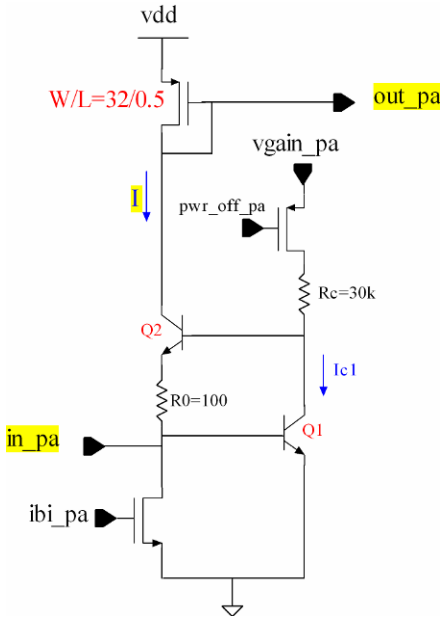


Figure 4: SBC preamp

The output of the current conveyor is copied by 6 variable size switchable current mirrors (Fig. 5) to allow a 6bits gain correction (Gain=2, 1, 0.5, 0.25, 0.125, 0.06) per channel. The 64 times 6bits are loaded in the integrated slow control register.

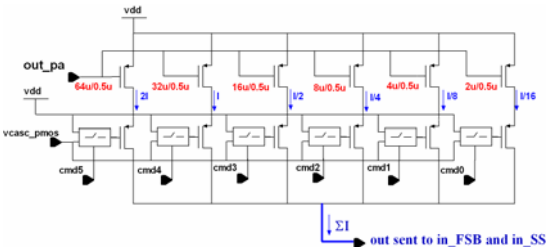


Figure 5: Gain correction

B. *Slow channel*

The slow channel is made of a variable peaking time CRRC shaper followed by a 2 pF and a track and hold buffer to deliver a multiplexed charge output (5MHz), which is useful for detector characterisation

Fig.6 shows slow shaper waveform for an injected charge of 1 and 10 pC. Its gain is about 80mV/pC and the peaking times car be varied between 75 and 150ns.

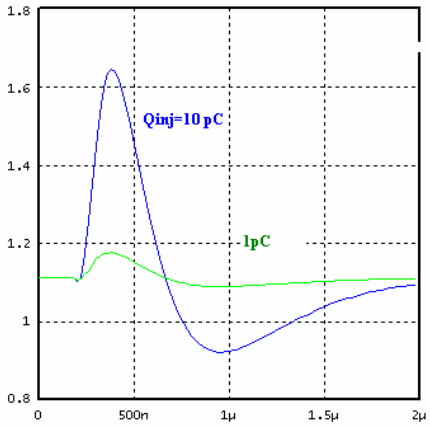


Figure 6: Waveform of the slow shaper

C. *Fast channel*

The fast channel is made of a variable gain and peaking time fast shaper (Fig. 7) followed by 2 discriminators.

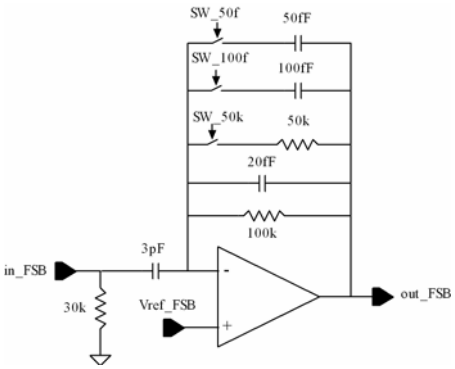


Figure 7: Bipolar Fast Shaper

The Fig. 8 displays the fast shaper waveforms when 100fC are injected. Its largest gain is about 3.5mV/fC and its fastest peaking time is equal to 15ns. The reference voltage Vref_FSB (equal to 2V) is referred to a 2.5V integrated bandgap as well as all the references used in the chip, to ensure their stability.

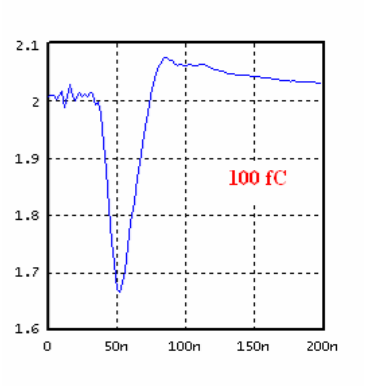


Figure 8: Bipolar Fast Shaper waveform

The DC uniformity (Fig. 9) of the 64 channels is 1.2 mV.

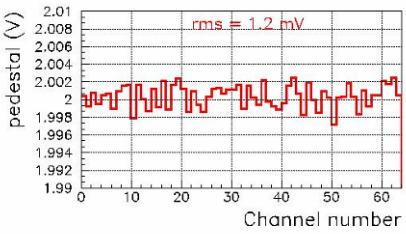


Figure 9: DC FSB dispersion

The analog crosstalk (Fig.10) has been measured by sending 100fC in one channel and looking to the direct neighbours. This 2% crosstalk is well differentiated and located on the input. It has been also checked that there is no long distance crosstalk.

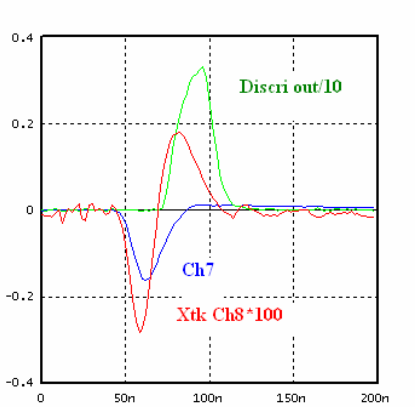


Figure 10: Crosstalk measurement

The linearity of the 2 10 bits integrated DACs used to generate the thresholds of the discriminators, has been measured: the residuals of both DACs are within ±5 mV for a 2.6V dynamic range which corresponds to an Integral Non Linearity of 0.2% (2LSB). The slope is 2.5mV per DAC unit.

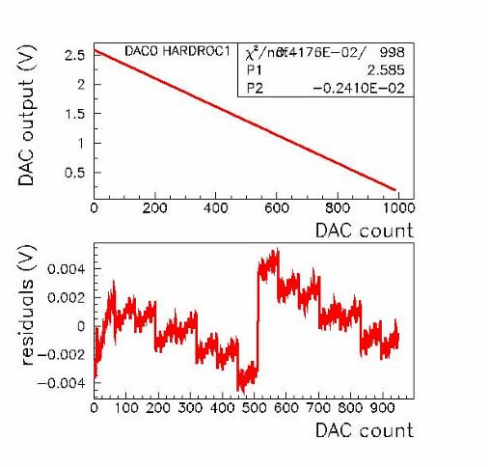


Figure 11: DAC linearity

The Figure 12 represents the s-curve measurement performed on the 64 channels of the chip. A charge of 100fC is injected and the threshold voltage is varied between 0 and 200fC. The quite large non uniformity between channels (±25 %) is explained by current mirror mismatch (small size transistor to optimize speed) but this can be corrected using the gain tuning of the input preamp. The resulting dispersion after gain correction is ±5%.

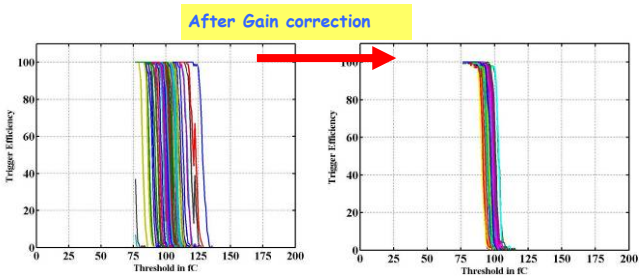


Figure 12: Trigger efficiency

D. *Digital part*

Because of the very high number of electronic channels foreseen in the final detector, chips will be embedded inside the detector and are designed to be daisy chained (Fig. 13) without any external circuitry, to limit to a bare minimum the number of output lines on the detector.

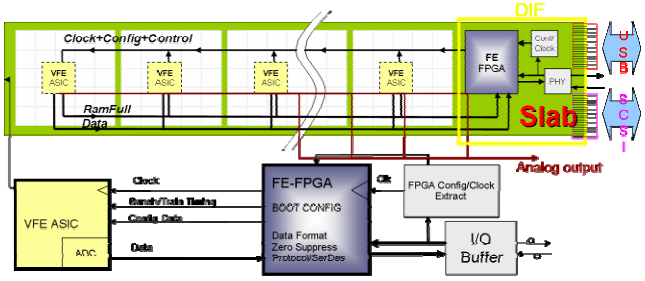


Figure 13: Daisy chain

A memory has been integrated in HARDROC to store during the bunch train the 2bits trigger outputs of each channel as well as the BCID, and this for every hit. The digital signals can be daisy chained and are open collector. There is the possibility to use either the internal signal (OR of the 64 channels) either an external trigger (Fig. 14).

The data format is 128(depth)*[2 bits * 64 ch + 24 bits (BCID) +8 bits (header)] =20kbits. There is one serial output which is transferred to the DAQ during the interbunch.

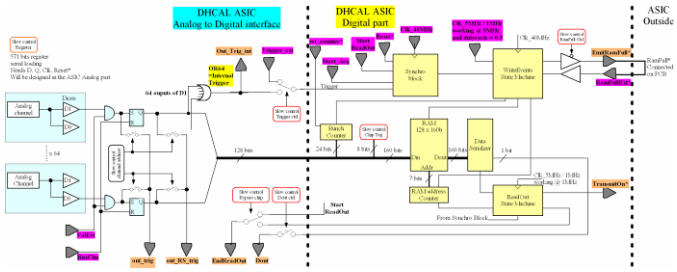


Figure 14: Digital part

The Figure 15 displays a memory frame. The auto trigger mode which is crucial for the chip functionality has been checked successfully down to 10fC.

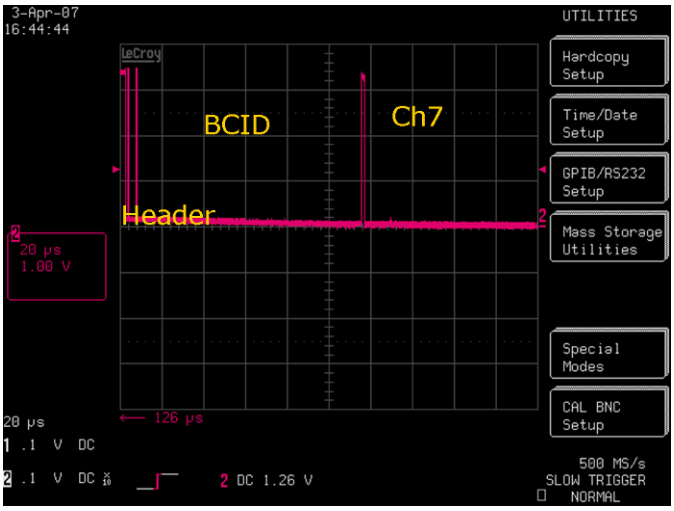


Figure 15: Auto trigger mode with 10 fC

The trigger crosstalk has been measured (Fig.16) by injecting a charge in one channel (Ch7) and measuring the trigger efficiency on the direct neighbours. There is no crosstalk for injected charge lower than 1.6pC.

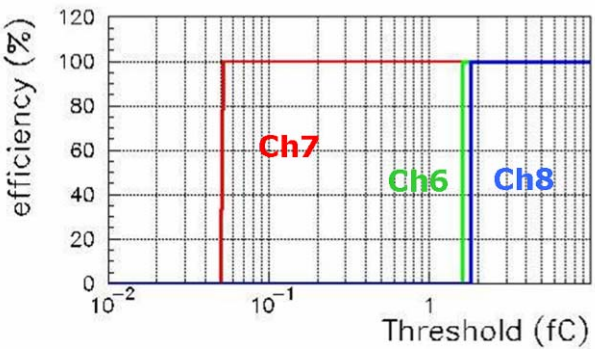


Figure 16: Trigger crosstalk

E. Power pulsing

To minimize the power consumption the chip is fully power pulsed by interrupting the bias current of the different cells during the interbunch.

The power dissipation (table 1) has been measured without the power pulsing for each cell:

Table 1: Power summary for 64 channels

Preamp	6 mA	100µA/ch
Bipolar FS	5.3 mA	
2 discri.	5.9 mA	
DAC	0.8 mA	
Bandgap	5 mA	
Digital part	3 mA	
Slow Shaper	14.5mA	For debug only

The total dissipation is 140 mW if the slow shaper is used and 90 mW without the slow shaper for 64 channels ie 1.4mW/channel, which is reduced to 8-15 µW/ch using the power pulsing (0.5 to 1% duty cycle).

IV. NEXT STEPS:

A PCB hosting four HARDROC (Figure 18) has also been designed to study the signal connection between the different chips before extracting it through a USB device. The PCB board will be associated to both RPC and µMEGAS detectors in order to validate the whole concept through exposure first to cosmics and then to beam test at CERN.

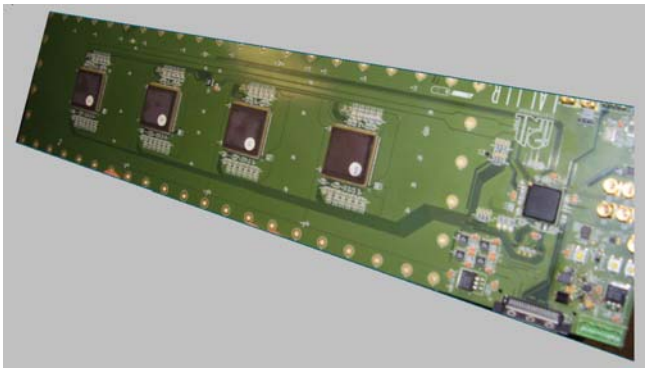


Figure 17: PCB with 4 packaged HARDROCs

V. CONCLUSION

All the tests performed have showed a good performance of the chip (summary in table 2) which allows to mount it on the detector that will go on test beam. HARDROC will allow developing the 2nd generation DAQ of CALICE-EUDET and testing a digital hadronic calorimeter based on RPCs, GEMs or Micromegas.

Table 2: HARDROC performance summary

Number of inputs/outputs	64 inputs, 1 serial output
Input impedance	50-70Ω
Gain adjustment	0 to 4 bits, accuracy 6%
Bipolar Fast Shaper	3.5mV/fC, tp=15ns
10 bit-DAC	2.5mV/fC, INL=0.2%
Trigger sensitivity	Down to 10 fC
Slow Shaper	80 mV/pC, 5fC to 15 pC, tp=75 ns to 150ns
Analog Xtk	2%
Analog Readout speed	5MHz
Memory depth	128 (20kbits)
Digital readout speed	5MHz or more
Power dissipation (not pulsed, without Slow Sh)	100 mW (64 channels)

VI. REFERENCES

[1] web site: http:/elec-in2p3.lal.in2p3.fr/micro/hardroc/

[2] System aspects of the ILC-electronics and power pulsing Talk at this workshop made by P. Goettlicher for the CALICE-collaboration