A Data Readout Module for the TOTEM Experiment

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Abstract

A general overview of the electronics system for TOTEM experiment is presented, and its connection with the CMS DAQ and control systems. The work on the data readout module for digital data is described more in detail, with its compatibility requirements with CMS, where it could serve for the CMS preshower detector, and its flexibility to read out digital data from different detectors. The design strategy, the data format and the front-end interface to the detectors is described.

I. Introduction

TOTEM (Total Cross Section, Elastic Scattering and Diffraction Dissociation) [1] is an experiment dedicated to the measurement of total cross section, elastic scattering and diffractive processes at the LHC. The full TOTEM detector consists of Roman Pot Stations (RPS), Cathode Strip Chambers T1 (CSC) and Gas Electron Multipliers T2 (GEM). The T1 and T2 detectors are located on each side of the CMS interaction point in the very forward region, but still within the CMS cavern. Two Roman Pot stations are foreseen on each side of the interaction point at 220 m and 150 m. Each Roman Pot station consists of two groups of three Roman Pots at a distance of a few meters to obtain a sufficiently large lever arm to establish co-linearity with the LHC beam for the tracks prior to generating a level one trigger for the corresponding event. Each Roman Pot contains 10 silicon strip detectors with 512 strips read out by 4 VFAT readout chips.

Future experiments in High Energy Physics, such as TOTEM for the LHC at CERN, raise the demand for high performance data processing and Data Acquisition Systems (DAQ). Multilevel filtering DAQ architectures require fast buffering for intermediate storage of raw data while the event is processed in various levels.

II. General specifications

General requirements are that the three TOTEM detectors should be able to operate as a sub detector of CMS. They need to provide trigger inputs which are in time to generate a global trigger for the CMS experiment, which is particularly difficult for the Roman Pots at 220 m from the interaction point. The detectors should be triggered by the general CMS trigger, and their data should be incorporated into the CMS data acquisition.

A. Trigger partition and trigger generation

TOTEM will be allocated one timing partition out of 32. It will receive its trigger and timing information for all three detectors from this partition. The Timing, Trigger and Control (TTC) system adopted is the one developed in common for all LHC experiments. Events are

synchronized with the 40.08 MHz bunch-crossing clock of the LHC machine. Currently it is foreseen that TOTEM provides 16 inputs out of 128 to the global trigger box of CMS. Of these 8 are allocated to the Roman Pots, 4 to the T1 detector and 4 to the T2 detector. The trigger signals are generated independently for the three TOTEM detectors. Whether they are forwarded as such to CMS or first put into coincidence prior to sending them to CMS is still under discussion.

Because of the stringent latency requirement on the trigger coming from the Roman Pots at 220 m a special rack was foreseen at an optimal location in proximity of the global trigger box of CMS while minimizing the cable length. Apart from the electronics treating the trigger signals coming from the TOTEM detectors, this rack will also house part of the readout cards of the Roman Pots and perhaps also of T2 and T1 detectors.

III. TOTEM electronic system architecture

The architecture of the TOTEM electronic system is shown in Figure 1. The TOTEM electronic system contains the following general components: Front End Electronics (FE), Optical Interface to Front End Driver (FED), Parallel Interface (S-Link64) and Front End Link (FRL) to CMS DAQ system. In an effort to standardize across different detectors, TOTEM opted to use the same front end chip (VFAT) in several detectors. The VFAT [6] will be used in the Roman Pots and in the GEM detector (T2) and might be used as well in the CSC detector (T1). The VFAT chip is read out by means of the Gigabit Optical Link (GOL) chip. Both components were developed in the MIC group at CERN: the GOL chip has been around in final form for some time; a new version of the VFAT is currently under development and will be submitted for fabrication soon. The GOL chip which serializes data can operate at 800 MHz or 1600MHz (for effective data rates of 640 Mbit/s and 1280 Mbit/s) and can drive a laser for an optical link.

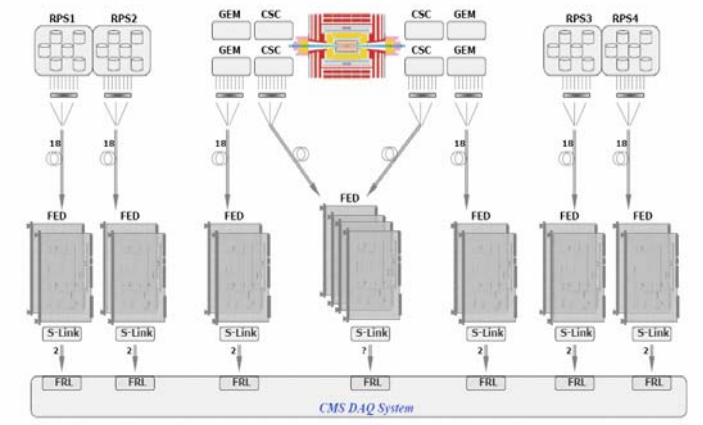

Fig. 1. TOTEM Electronic System

The VFAT has been designed in 0.25μm CMOS has two basic functions. The first (Trigger) is to provide fast regional hit information to aid the creation of a LV1 trigger and the second (Tracking) is for providing precise spatial hit information for a given triggered event. It has 128 identical channels. The VFAT will read out the majority of the TOTEM detector channels, but on some channels other CMS read out chips are being considered (for instance the APV [7] chip for analogue read out of the strips in the GEM detector).

IV. Data readout mobile

The CMS data acquisition system contains 512 legs (Front End Readout Link or FRL [4] of which some fraction will be allocated to TOTEM. Each of these FRLs is capable of taking a maximum average data rate of 200MByte/s or 2kByte/event at a maximum LV1 trigger rate of 100 kHz. Based on data rates 8 FRLs will be located to the Roman Pot system, 7 to T2 (2 for APV, 5 for VFAT), and 6 for T1. The maximum level one trigger rate foreseen for CMS (which determines the data rate through the FRLs) is 100 kHz.

A. Functional Block Diagram

The FED functional blocks are shown in Figure 2. The general blocks are: Optical Receivers (Opt RX), Deserializers (DES), Input Handler, Event Memory (MEM), Event Builder (EB), S-Link64 [2] interface, VME64x interface and Spy Memory. After optical to electrical conversion by Opt RX and deserialization by DES, input data is stored by Input Handler in the input memories.

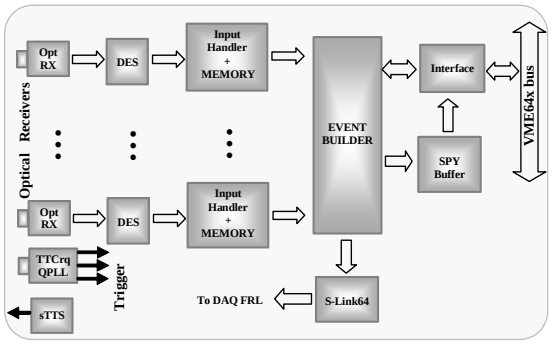

Fig. 2. FED Functional Block Diagram

Event Builder collects the data fragments from the group of 12 optical channels, builds the event and sends to three separate S-Link64 interfaces. 32MByte Spy memory buffer is using for local monitoring via VME64x.

The CMS ECAL group has developed the Data Concentrator Card (DCC) [3]. The board has 72 optical 800 Mbit/s inputs implemented in 6 NGK 12-Channels Receivers.

This board is very close to the full GOL count for the Roman Pots (72) and about twice the GOL count of the GEM detectors. However, the information content of the TOTEM GOLs is much higher, and does not allow to fully equip one card (which only interfaces to one FRL). The totem data density allows one S-link64 (and one DCC) to cover 9 optical channels only. Therefore a new module is being designed using the previous development as much as possible.

B. Module Design Strategy

The Data Readout Module is being designed in modular form. It is built from a set of mezzanine cards plugged onto a main motherboard. The expensive optical components are mounted solely on mezzanine cards, so that they can be tested separately and preserved if the motherboard is defective. Motherboards can be equipped with a fraction of the total number of mezzanines, and some of the mezzanines can be different depending on the application. In particular, for the CMS preshower application it is possible to associate the same number of incoming fibres to only one FRL using a mezzanine card which does advanced zero suppression and pedestal subtraction to reduce the data, while for the TOTEM application the incoming data is distributed over three FRLs. The board is intended for operation in a VME

environment in the experiment but is also equipped with USB ports to allow standalone operation. This is being implemented largely based on previous CMS preshower work [8].

A general overview of the boards is presented in Figure 3.

The motherboard is in 9U VME64x format. It contains VME64x interface chip and Local Bus controller; three Event Builders; Spy Memories; hosts for three Optical Modules (OM), see [8], three USB2.0 controllers, a FEC mezzanine board for standalone operation outside the experiment, Local Trigger Board, and TTCrx .

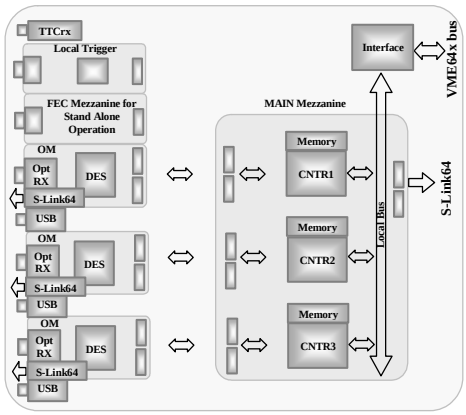

Fig. 3. FED Block Diagram

On top of every OM board is possible to plug-in S-Link64 transceiver board, which connects the readout module to the DAQ system. There is fourth S-Link64 interface on the VME J2 connector and additional rear adapter. Event Builders received data, builds the event in corresponding format and transfer it to the S-Link64 controllers. The Spy Memories associated with every event builder are using to spy on request the event data. Slow readout is possible via VME or via USB buses. Interface to the CMS DAQ system is via S-Link64 interface and FRL. Main mezzanine board is connected between Local Bus, S-Link64 interface and Optical Modules. To implement all the functions and controllers, latest generation Field Programmable Gate Area (FPGA) are used. The VME64x controller is implemented in Cyclone™ device from Altera. Event Builders are in Stratix™ GX, which has multiple gigabit transceiver blocks, each with four full duplex channels. Using clock data recovery (CDR) technology, these channels serialize or deserialize data for transmission rates up to 3.125 Gbps.

V. Data format

Data from TOTEM detectors presented to the module optical inputs is formatted by VFAT chip. The format is defined as in Figure 4.

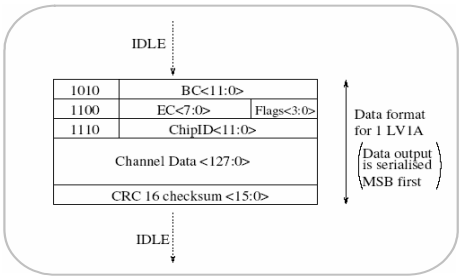

Fig. 4. Data Format

Total length is 16 bits, where: BC<11:0> is Bunch Counter number; EC<7:0> Event Counter; Flags<3:0>; Chip ID<11:0>; Data<127:0>; CRC 16 checksum<15:0> and four control bits for the beginning of the frame. For multiple triggers frames are following one after the other for every LV1A request.

When an event fragment is ready to be transmitted to the DAQ, the FED encapsulates the data according to the common CMS data format [5] shown in Figure 5 and writes the data into the corresponding S-Link64 port.

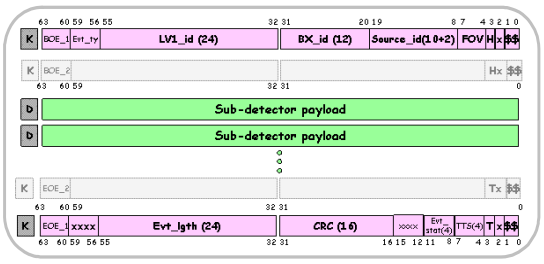

Fig. 5. CMS Common Data Format

The encapsulation words are control words flagged by the S-LINK64 control bit. Detector payloads are data words.

Field definition is following:

- *BOE_n*: Identifier for the beginning of an event fragment (BEO_1 = hex 5);
- *Evt_ty*: Event type identifier;
- LV1_id: The level-1 event number generated by the TTC system;
- BX_id: The bunch crossing number. Reset on every LHC orbit;
- *Source_id*: Unambiguously identify the data source (FED/DCC): 2 bits reserved for FED internal;
- *FOV*: Version identifier of the FED data format;
- *H*: when set to '0', the current header word is the last one. When set to '1', another header word is following;
- *EOE_n*: Identifier for the end of an event fragment (EOE_1 = hex A);
- *Evt_lgth*: The length of the event fragment counted in 64-bit words including header and trailer;
- *CRC*: Cyclic Redundancy Code of the event fragment including header and trailer;
- *Evt_stat*: Event fragment status information;
- *TTS*: Current values of the TTS bits;
- *T*: when set to '0', the current trailer word is the last one. When set to '1', another trailer word is following;
- *x*: Indicates a reserved bit;
- *$*: Indicates a bit used by the S-LINK64 hardware.

VI. Module layout

The layout of the module is shown on Figure 6. As the module is on layout stage this represent preliminary placement of the components and the mezzanine boards.

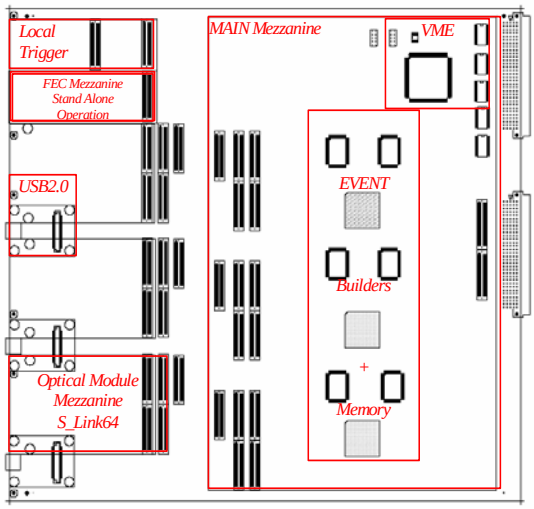

Fig. 6. FED Layout

VII. Conclusions

The data readout module follows closely the requirements of the TOTEM electronics system and is therefore a fundamental element. It can also equipped with an additional mezzanine for advanced data reduction and pedestal supression for the CMS preshower detector which has a completely different raw data density. With reprogramming and an additional mezzanine on motherboard, it can also be used as a VFAT emulator to test the entire readout chain. The module is intended to operate in a VME environment in the experiment but can be used in a standalone environment using USB and PC.

VIII. Acknowledgements

The authors would like to thank Joao Varela (LIP Lisbonne, Portugal) for his support and ideas and also Georgios Sidiropoulos (University of Ioannina, Greece) for participating into the idea of building a FED card based on plug-in modules.

IX. References

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