The High Voltage Distribution System for The Hybrid Photodetector Arrays of RICH1 and RICH2 at LHCb

C. Arnaboldi, T. Bellunato, T. Gys, E. Panzeri, G. Pessina, and D. Piedigrossi

***Abstract*—Two Ring Imaging CHerenkov detectors, RICH1 and RICH2, will provide the particle identification of the LHCb experiment. The Cherenkov light cones produced in three different refractive media are projected onto four arrays of Hybrid Photon Detectors (HPDs), with 484 HPD units in total. In order to accelerate and focus the photoelectrons resulting from the conversion of photons in the HPD photocathode, the electron optics of an HPD requires three different high voltages (HVs): -20 kV, -19.7 kV and -16.4 kV. We describe in this paper the HV distribution system that has been designed for this purpose. The HV is supplied by printed circuit boards specially developed to prevent electrostatic discharges and/or Corona effects across the volume of the HPD arrays. The circuits allow for the splitting, distribution, protection and monitoring of the high voltages. Each board is covered with silicone rubber, which prevents electrostatic breakdown, and a study has been made on its radiation tolerance. A prototype HV system has demonstrated compliance with all experimental requirements. Finally, a production test system has been implemented to provide for a precise characterization of each HV board, in order to guarantee optimal yield.**

***Index Terms*—HV distribution system, HV photon detector biasing, silicone insulation.**

I. Introduction

PARTICLE identification in the LHCb experiment [1] will be performed by two Ring Imaging Cherenkov Detectors, RICH1 and RICH2. The RICH detectors [2] contain three radiator materials, optimized for the charged-particle momentum they are required to discriminate. The cones of photons produced by the particles will be reflected by two sets of spherical and flat mirrors onto arrays of Hybrid Photon Detectors (HPDs) [3], placed outside the acceptance of the LHCb spectrometer. The HPDs are mounted on a column structure. RICH1 will have 196 HPDs, arranged in 2 arrays, each with 7 columns of 14 HPDs per column. RICH2 will have 288 HPDs, also arranged in 2 arrays, each with 9 columns of 16 HPDs per column. The area covered by both arrays of HPDs is about 2.6 m^2; the active diameter of a single HPD photocathode is 72 mm.

The photoelectrons produced by incident photons converted in the HPD photocathode are accelerated and focused by a cross-focusing electrostatic field onto a silicon pixelated anode. Three high voltages (HVs) are required for the electron optics: -20 kV, -19.7 kV and -16.4 kV. At the silicon anode, the electrons are detected and read out with a granularity of 32×32 into a CMOS pixel readout chip, each channel containing an amplifier-discriminator network. A 40 MHz binary readout of the signals from each pixel is then performed and the data are transmitted via optical fibre to the control room. The front-end readout, its voltage biasing and the HPD HV distribution are located on the columns which also have mounted the HPDs.

In this paper we will describe the distribution scheme which delivers HV to the HPDs of both RICH detectors. This consists of a series of HV circuit boards specifically designed to provide the three bias voltages, including protective networks. An accurate test system has been developed to fully characterize the boards. The layout includes an "analogue boundary scan" to perform accurate characterization and testing.

The maximum radiation levels across the HPD regions are expected to be about 30 kRad (Total Ionizing Dose—TID) and 3×10^{12} n/cm^2 (1MeV equivalent Non-Ionizing Energy Loss—NIEL) over the ten years of running. These values include a safety factor of 2. We have therefore tested the radiation-hardness properties of most of the components used and some prototype boards covered with the insulator "Silicone Tough Gel".

II. Circuit Set-Up

A. Overview

Every HPD column is segmented in two half-columns for the distribution of HV biasing. The half-column unit is therefore the minimum part of the detector to be disconnected in case of malfunction. The -20 kV HV supply voltage to each half-column is delivered from the control room via a 100 m-long cable, and is then fed to its individual -20 kV input located in the middle of the column.

A half-column consists of 8 HPDs in RICH2. In RICH1, which has 14 HPDs per column, there are 6 and 8 HPDs respectively in every alternate half-column. The HPDs are biased in pairs; in this way 3 or 4 HV boards measuring 90×165 mm^2 are mounted side by side along the column, the longer side parallel to the column. As an illustration, Fig. 1 shows the layout diagram of a half-column of RICH2. The three HV lines are generated by a potential divider network on the board at the end of the half-column, and then daisy-chained from board to board. The functionality of the system of boards is represented in the schematic of Fig. 2, where V_1, V_2 and V_3 are the 3 HVs, -20 kV, -19.7 kV and -16.4 kV, respectively.

There are two distinct types of board, designated S and M, which have differing designs of the blocks labeled "Splitter" and "Monitoring." The main input supply to the boards, fed into the Splitter block, is -20 kV. This block generates the three HV values to be distributed. The block labelled "HPD bias" provides

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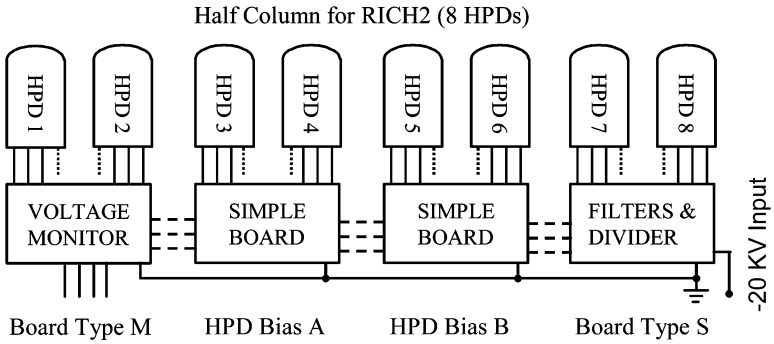

Fig. 1. Half-column layout of RICH2.

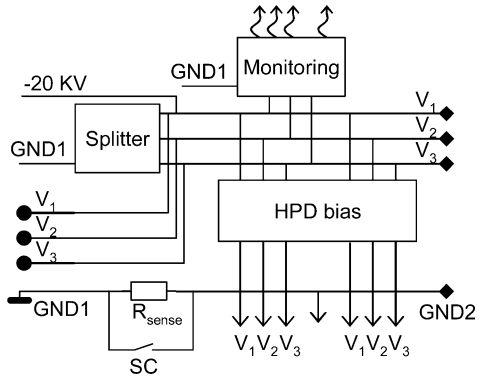

Fig. 2. Schematic diagram of an HV board.

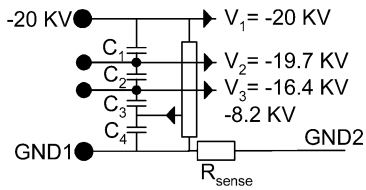

Fig. 3. Schematic of the Splitter block of Fig. 2.

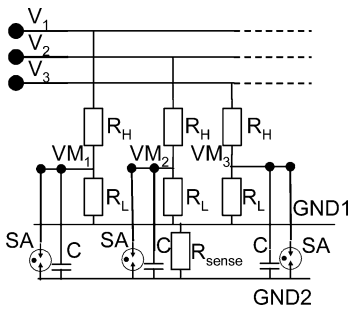

Fig. 4. Schematic of the Monitoring block of Fig. 2.

the HV distribution to a pair of HPDs, and this component is the same for every board. The "Monitoring" block provides low voltage outputs for external monitoring of the HV values.

The space available for the electrical components is small, given that a resistor rated for 20 kV is about 5 cm long. Consequently, the Splitter and Monitoring blocks cannot both be contained in the available board space together with the HPD bias block. Therefore we have one Splitter and one Monitoring board per half-column, located at each half-column end. Within the half-column there is either one (RICH1) or two boards (RICH1 and RICH2) that do not need the presence of either the Monitoring or Splitter blocks. For the boards in the centre of the half-column, either Type S or M boards are used, but populated only with the HPD bias block. The detailed functionality within each of the blocks of Fig. 2 is described below.

B. Circuit Description

The circuit design for the splitter block is shown in Fig. 3. It consists of a custom resistive divider (Manufactured by Ohmcraft, http://www.ohmcraft.com), connected in parallel with HV filtering capacitors (Murata, DHRB34C102 M2FB, http://www.murata.com/cap/). The splitter has a total resistance of $\sim$300 MΩ. Starting from the top of Fig. 3, the four resistor values in the splitter are 4.12 M Ω, 47.9 M Ω, 125 M Ω and 125 M Ω.

The HV capacitors act as filters. The values of C_1 to C_4 are 30 nF, 2.2 nF, 1 nF and 1 nF, respectively. The node between C_3 and C_4 has been added to the voltage divider to guarantee that the sharing of the HV between the two capacitors C_3 and C_4 is the same.

When the Type S board is fully populated, the inputs to the board are the -20 kV (V_1) and GND1. The outputs are the three voltages V_1 to V_3 and GND2, which are routed to the other blocks of the board and to the next board in the half-column. If the board is required only for biasing a pair of HPDs, the filtering capacitors and the voltage divider of the Splitter block are not mounted, and V_1, V_2 and V_3 and GND1 will be input at the nodes indicated with black circles on Fig. 3 (and Fig. 2).

The circuit design for the Monitoring block is shown in Fig. 4. It consists of a voltage splitter implemented with HV-precision 5 G Ω resistors, R_H, and 392 kΩ resistors, R_L. The resulting voltage range is centred on -1.57 V when, in normal operation, GND1 and GND2 are connected together. In this way, the HPD HV values can be monitored from nodes VM_i $(\mathrm{i} = 1, \ldots, 3)$. If the measurement system is not able to read out negative voltages, GND1 can be connected to a positive offset voltage in order to shift the voltage at the nodes VM_i accordingly. In parallel to each R_L resistor there is a 47 nF capacitance, C, and a 90 V surge arrestor, SA, to protect the outputs against any possible sudden discharge.

The board Type M implements both the Monitoring and HPD bias blocks of Fig. 2. If the board is required only for biasing a

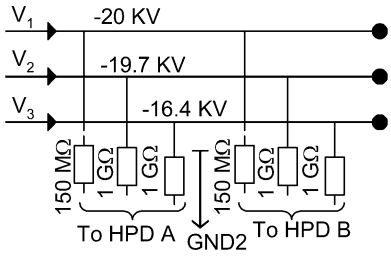

Fig. 5. Circuit diagram of the HPD bias block of Fig. 2.

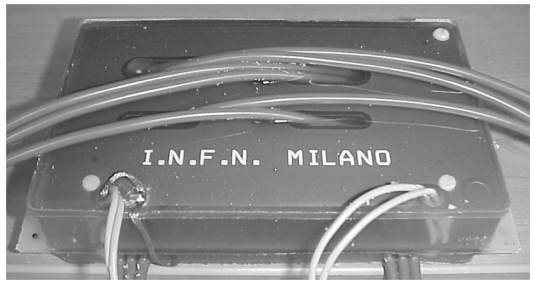

Fig. 6. View of an HV board when covered with STG with a shielding cover on the top (Cu shield is found just under the Solder Resist, where the Institution name is written).

pair of HPDs, the Monitoring block is simply not populated, in an analogous way to the Splitter block of the Type S board.

The schematic of the HPD bias block is shown in Fig. 5. It consists of a pair of three HV resistors in series with the HV lines, each one input to an HPD. The resistors prevent a large current flow in the case of an unexpected short-circuit to ground at any HPD bias node. The lower series resistor value on the cathode line (150 MΩ) makes provision for a possible increase of the dark photocurrent over the HPD lifetime. Both types of HV board include the HPD bias block of Fig. 5.

C. Analogue Boundary Scan

The Splitter block of Fig. 2 has a current consumption of about 67 μA, while the Monitoring block draws 11 μA. When the boards are tested after manufacture, we expect to measure a leakage current from the insulator material covering the board (see next section) in the nA range, i.e., much smaller than the currents drawn by the Splitter and Monitoring chains. To be sensitive to the measurement of the leakage current, we have laid out the boards in such a way that the ground can be split, during the test phase, to allow for separate monitoring of the Splitter or Monitoring currents from the insulator current. This is made possible with the resistor R_{sense}, as shown in Fig. 2, in conjunction with a proper board layout. The reference ground for both types of boards, S and M, is GND1. The Splitter and Monitoring blocks are laid out in close proximity to the location of R_{sense}. This ensures that the current flowing in GND1 is the one from the Splitter or Monitoring blocks, while the very small leakage current coming from the rest of the PCB will flow through GND2, developing a small, but measurable, voltage drop across R_{sense} (200 k Ω). GND2 is a sensitive probe since it is a track routed through the whole length of the board and the monitoring of this node is very important to control and test the quality of the board.

During normal operating conditions, R_{sense} is short circuited and GND1 and GND2 become the same low impedance path.

III. Board Layout and Insulation Protection

The electrical components to be used in HV applications have large dimensions and the distance between nodes biased at very different potentials should respect minimal values. For the RICH HV boards, the available space is limited and the components used are restricted to be within close proximity. For this reason, many precautions have been taken to achieve adequate performance.

Although the electrical circuit is not complicated, we have laid out the PCBs with 4 layers to embed all tracks in the inner layers: the HV tracks just under the top layer, the tracks of lower potential just above the bottom layer. Between any tracks and the closest surface there is 0.8 mm thickness of fibreglass. Exceptions to this are the solder pads where special precautions, described below, have been taken.

To avoid discharges between nodes at very different potentials, the boards are completely enclosed in the insulator material Silicone Tough Gel, STG (Sylgard DC 3-4241 by Dow Corning, http://www.dowcorning.com/). This material has a dielectric strength in excess of 17 kV/mm, compared with dry air that is close to 3 kV/mm. The use of STG therefore allows a considerable saving in the minimal compliance distance to be held between components. STG is a proven long-life material in outdoor applications and in very adverse environmental conditions [4]–[22]. It is therefore a very adequate protective material, durable for the lifetime of the LHCb experiment. The thickness of STG on the top of the board is 18 mm in order to fully coat the electrical components, while on the bottom of the board the thickness is 8 mm.

Fig. 6 shows a photograph of a completed HV board, coated with STG, and having a copper top cover (that appears green, the colour of the solder resist) connected to ground for shielding purposes. An equivalent cover is also implemented at the bottom.

After population of components, the board is cleaned with trichloroethylene, and subsequently mounted in a mould made from aluminium covered with PTFE. The mould is then filled with liquid STG and placed in a vacuum chamber for about 20 min at about 0.2 mbar pressure, to eliminate bubbles that can impair the dielectric strength. After this, for about 3 h, the mould is placed in an environmental chamber at 60°C, to cure the STG. During this time, the STG solidifies and the mould can then be removed. The board temperature is then maintained at 60°C for at least 4 days to anneal. We have observed that the leakage current remains larger than expected if such a long annealing time is not respected. This is because the residual ions trapped in the rubber bulk need a very long time to migrate outside the bulk at room temperature.

Since the tracks are embedded under the PCB fibreglass, the leakage current in the STG can only originate from the soldering pads towards the top and bottom covers and parallel to the surface of the PCB, where the resistivity is much lower than in the

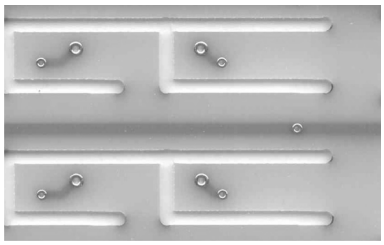

Fig. 7. Expanded view of part of the PCB, in the region of some solder pads.

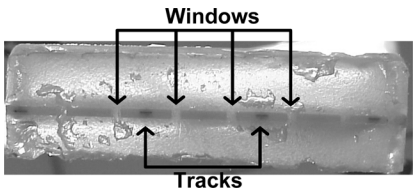

Fig. 8. Cross-section of the board covered with the STG. Arrows on the top indicate where the air indents are filled with STG.

bulk rubber. We have improved the surface effects by layout optimisation. In the PCB we have created "air indents" with widths that range from 2 mm to 5 mm, which separate the solder pads and the critical tracks. This layout is shown in Fig. 7. When the STG fills the air indents, the electric field parallel to the surface experiences an orthogonal barrier that has a strong dielectric strength, more than 34 kV/mm. This method solved completely the initial failures resulting from surface effects, which were almost the only source of observed defects.

Fig. 8 shows the cross-sectional view of a board covered with STG. The arrows indicate where the STG surrounds the tracks, making the dielectric strength almost isotropic. The parallel field strength is considerably reduced when an air indent filled with STG is encountered.

We will now quantify the expected leakage current from the STG. If we assume that the dimension of a solder pad is much smaller than the distance between any other pads, we can approximate the resistance between the pad and any other point at a different potential by the expression [23]

$$\mathrm{R_{Pad}} \approx \frac{\rho}{\pi a}. \tag{1}$$

Here ρ is the STG bulk resistivity, of the order of 3×10^{15} $\Omega\cdot$ mm for the Sylgard DC 3–4241, and a is the linear dimension of the pads, assumed to be approximately circular. This approximation is valid as long as the position of the node that sinks the current is far from the pad, as is the case with the covers and the track GND2. For a given board, there are about 45 pads, each having a diameter between 2 mm and 3 mm, held at various values of HV. Using approximation (1), the current that leaves the smaller pad at the lower HV value of 8.2 kV is about 17 pA, whilst from the larger pad at 20 kV it is about 63 pA. Summing up the currents from every pad we roughly estimate about 7 nA of total leakage current.

During the characterization phase we connected the top and bottom shields to GND2. Therefore, the sum of the currents will flow through resistor $\mathrm{R_{sense}}$ from these three so-called "sinking nodes." Fig. 9 shows the result of a measurement from a board type S over three days. During the measurement period the HV was cycled from -20 kV to zero once per day. It can be seen that although the standing current coming from the splitter is more than 60 μA, the current measured with the active analogue boundary scan is in the nA range, consistent with the extrapolation obtained from (1).

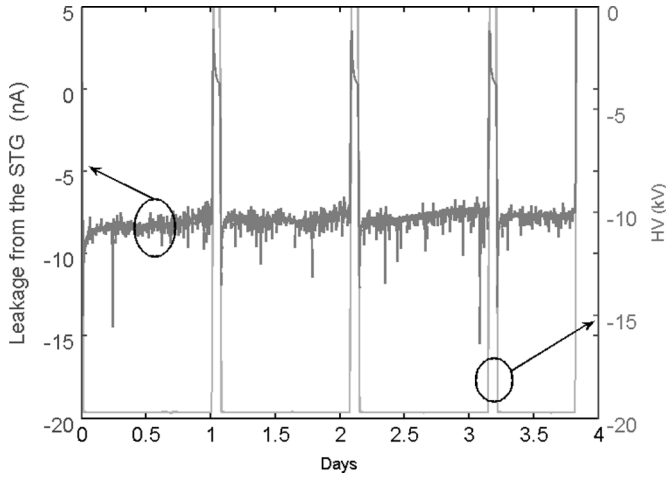

Fig. 9. Long term measurement of the leakage current from the STG, (left axis). with the HV cycled once per day (right axis).

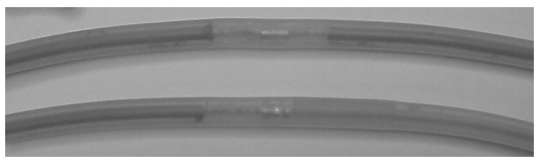

Fig. 10. Examples of HV cable connections.

IV. Cable Connections

To connect the HV cables from PCB to PCB and from PCB to HPDs, we have used small brass cylinders where the pairs of wires to be joined are internally soldered. After the wires are joined, an insulating tube covers the connection point. The tube is made with commercial silicone having 2 mm thickness and about 18 cm length, adequate to cover the connection. Fig. 10 shows examples of such connections.

V. Radiation Hardness Investigation

The maximum radiation levels across the HPD regions are expected to be about 30 kRad (Total Ionizing Dose—TID) and 3×10^{12} n/cm^2 (1MeV equivalent Non-Ionizing Energy Loss—NIEL) over the ten years of running. These values include a safety factor of 2. We carried out an irradiation test of the HV boards at the GIF irradiation facility at CERN (http://irradiation.web.cern.ch/irradiation/) in November 2004. Most of the electrical components used to populate the boards and two complete boards were subject to a particle flux composed of neutrons and γ s (90%) plus protons and pions (10%) for a total fluence of 3×10^{12} n/cm^2 (1 MeV equivalent). As already mentioned above, this fluence corresponds to the maximum one expected after 10 years of operation at the location of the

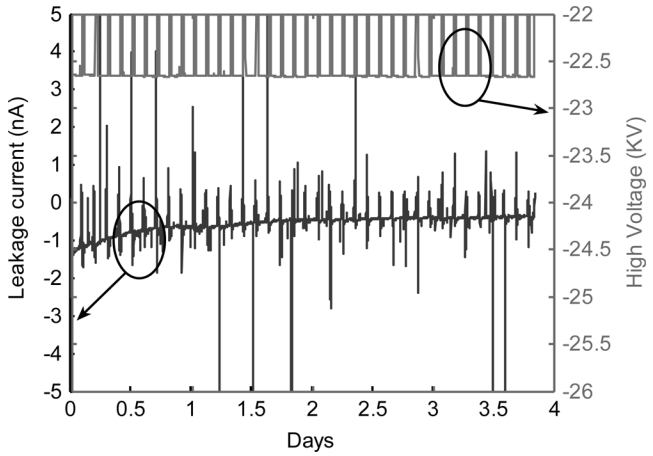

Fig. 11. Leakage current from a board before irradiation.

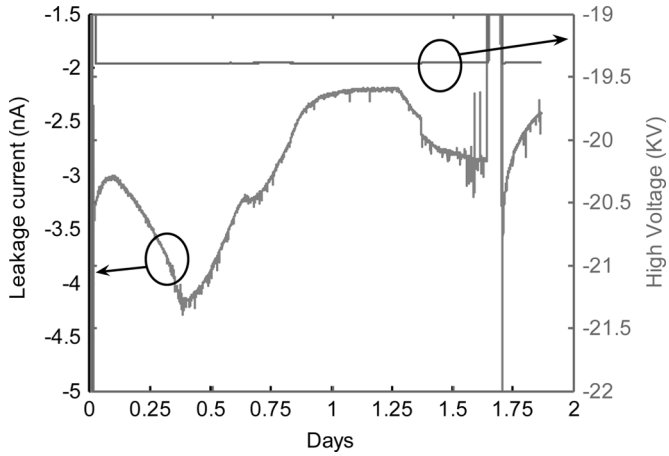

Fig. 12. Leakage current from a board after irradiation.

HPDs and includes a safety factor of 2. After irradiation, there was no change in the electrical characteristics of the resistors. The capacitors were also found to be stable, although the 10 nF devices increased their value by somewhat less than 10%.

The leakage current from a complete board, measured before and after irradiation, confirmed the characteristics of the electrical components and proved also that the selected STG is adequate for this application. We compare in Figs. 11 and 12 the leakage currents measured from a board before and after irradiation. (In this test the board was not equipped with the shielding covers on the top and the bottom and, as a consequence, we expected and measured, a level of current consistent with $1/3$ of that shown in Fig. 9, since only one sinking node was present). Whilst the average values differ, the values are compatible when taking into account the different conditions of the two measurements. Before irradiation the laboratory was under climatic control. After irradiation the measurements had to be made in a radiation-safe area where it was impossible to reproduce the same environmental conditions. In Fig. 12 the HV voltage applied is slightly smaller than that of Fig. 11 due to the different HV supplies available in the two laboratories.

An important item with HV integrity concerns the surface quality of the boards. If small apertures and/or cracks are created on the surface, a static high electric field can penetrate and create damage in the bulk. With STG it has been shown that this effect is highly inhibited under normal radioactive conditions and in a wild outdoor environment [24]–[27]. Fig. 13: shows a small region, zoomed 250 times, of the surface of the STG that covers one of the investigated boards, before irradiation. This is compared with the photograph of Fig. 14, taken after irradiation. There is no indication of a different surface aspect (cracks that may give rise to high electric field accumulation) that could be interpreted as a beginning of degradation resulting from irradiation.

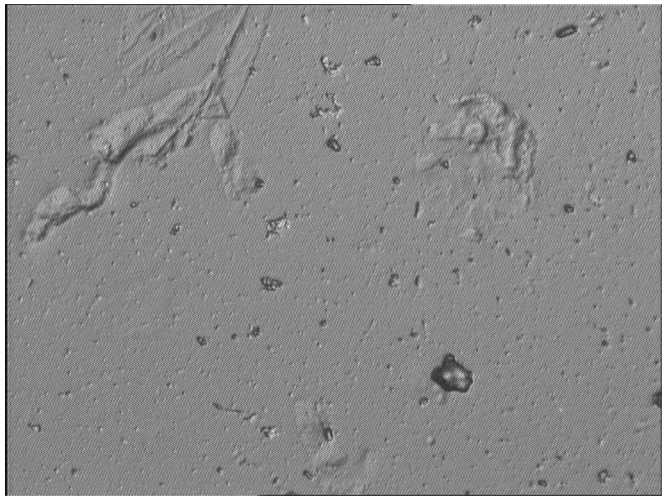

Fig. 13. Photograph magnified X250 of a small region of the surface of the Silicon Tough Gel that covers the board before irradiation.

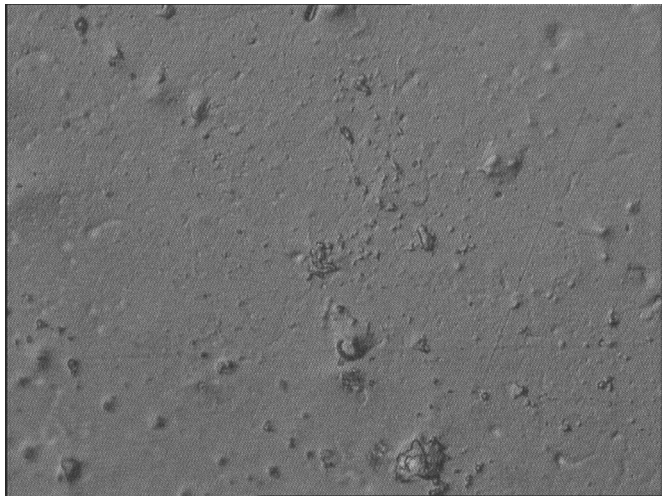

Fig. 14. Photograph magnified X250 of a small region of the surface of the Silicon Tough Gel that covers the board after irradiation.

VI. Conclusion

We have described the circuit design of the HV distribution system for the 484 HPDs of the LHCb RICH detectors. The splitter, monitoring and distribution schemes have been demonstrated. An analogue boundary scan to fully control the quality of the production of the HV boards has been described. The very small levels of leakage currents from the STG used to fully coat the boards has been measured, superimposed on the bias current. The HV boards and components have been exposed to a fluence

of 3×10^{12} n/cm^2 (1 MeV equivalent). No appreciable damage has been observed in the functional behaviour or on the surface of the insulator used to cover the boards. The design fulfils the requirements of LHCb and the HV boards will be installed in the final system during the coming year.

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